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Reduction of leakage power in CMOS circuits using efficient variable body biasing with bypass technique

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***Abstract*—Power leakage is one of significant issue in CMOS technology. So, to minimize the power leakage in CMOS circuits, there are various types of reduction approach have been proposed such as, Sleepy Stack, Sleep Transistor, Forced Stack, Zigzag etc. But In this paper, an efficient approach has been projected to minimize the dissipation of power in CMOS circuits i.e. efficient variable Body Biasing Technique in 45 nanometer CMOS technology. The proposed efficient variable body biasing with bypass (EVBB) technique gives better significant result than the previous existing leakage reduction techniques by reducing the time delay and area of the CMOS circuits. The propped EVBB technique requires less area and reduces maximum time delay of the proposed technique by incorporating the body biasing methods. In the proposed work, all the circuit design and simulation have been done by using MICROWIND software.**

Keywords*— *CMOS circuit, Power Leakage, EVBB, Sleep transistor.

I. INTRODUCTION

Now a day's leakage power is one of the solemn issues in CMOS VLSI circuits. The leakage power is increasing day by day due to decreasing device dimension. To overcome this leakage problem in CMOS circuits many researchers have been proposed numerous leakage reduction technique. But there is no universal way to solve this problem in CMOS technology. Thus, designers are required more accurate approach to solve this crucial problem in CMOS circuits and appropriately the result satisfy the applications and product needs. The leakage power of CMOS circuits encompasses both dynamic and static power dissipation. Now a days, as the technology is advances day by day so exponentially static leakage power is increases rapidly. So often it is said that the static power dissipation of a CMOS circuits is known as leakage power. Leakage power is a power which flows through transistor when it is in off position. According to International Technology Roadmap for Semiconductors (ITRS) [5] report gate leakage power will reach undesirable levels (mainly in battery operated devices) which are the key concern for new high dielectric materials in the field of low power and high-performance applications. Primarily, the power dissipation of a CMOS circuit is mostly depending on gate length, oxide thickness and varies exponentially with temperature, threshold voltage and other parameters. In the proposed work, an efficient variable body biasing with bypass approach has been introduced to reduce the power dissipation in CMOS circuits which gives better result than previous standard leakage reduction technique. The proposed technique is summarized and compared with the previous techniques which are reported in this work. The key components of leakage power in a CMOS circuit are shown in the Fig. (1) given below:

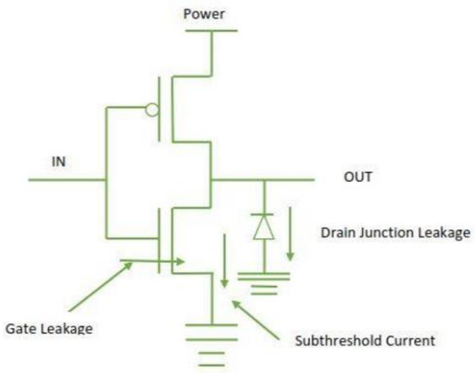

Fig. (1): Power leakage in CMOS circuit

II. RELATED WORK

Since last few decade, there are many researches have been done to reduce the leakage power in CMOS VLSI circuits by various researcher which are discussed in this section. To minimize the leakage power dissipation, various techniques has been proposed in CMOS circuits. But till now, there is no universal way to solve the leakage problem in CMOS technology.

A power reduction method has demonstrated [7,2] to minimize the power leakage in CMOS circuits which methods have ability to reduce the power leakage in CMOS better stability. In this paper a low power CMOS circuits had been described. Sleepy stack technique revealed in [6] to reduce the power dissipation in nano scale CMOS technology. They introduced Sleepy stack method to minimize the time delay as well as to make the CMOS Circuit area efficient because the sleepy stack circuit is nothing but the combination of forced stack and sleep transistor method.

A dual stack system [9] is developed to decrease the current leakage in CMOS circuits. The traditional sleep

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transistors method is used in dual stack technique to minimize the power dissipation in CMOS circuits. The dual stack method minimizes power leakage in CMOS circuits with smallest delay and area. A power reduction method [1] is successfully implemented which is called stack with sleepy keeper. The method has low V_{th} and high Vth which minimize the average power dissipation in CMOS technology. A power reduction method [10] was developed which is called sleep forced NMOS stack method to reduce the power dissipation in nano scale CMOS technology. The introduced method has less delay, good performance and area efficient. Variable body biasing with bypass technique [8] is introduced in 45 nanometer technology to minimize the power dissipation in CMOS circuit. Here, power efficient method has revealed to minimize the power dissipation in the CMOS circuits by incorporating with sleepy stack, sleepy keeper etc. technique. A power reduction method which is called body biasing technique is revealed in [11]. Here, body biasing method was used to minimize the power leakage in CMOS circuits by comparing with required area efficiency. The body biasing technique is estimated to control the total power consumption in CMOS circuit. Power minimization technique for CMOS technology which is known as zigzag with keeper is developed in [4]. The introduced technique is summarized from zigzag method and sleepy keeper approach. A V-body method [3] is introduced to decrease the power leakage in CMOS circuits. The described technique reduces stand by leakage power in nano-scale CMOS technology. The temperature and the supply voltage variants are compared by feedback loop in the introduced method.

III. PROPOSED WORK

In this section a new and efficient variable body biasing with bypass (EVBB) technique has been introduced to decrease the power leakage in CMOS circuit. The proposed parameters have been compared with the existing standard leakage reduction methods.

A. Efficient Variable Body Biasing with Bypass(EVBB):

To overcome the leakage problem in CMOS circuits, here VBB technique is used. The proposed EVBB technique is presented in Fig. (2).

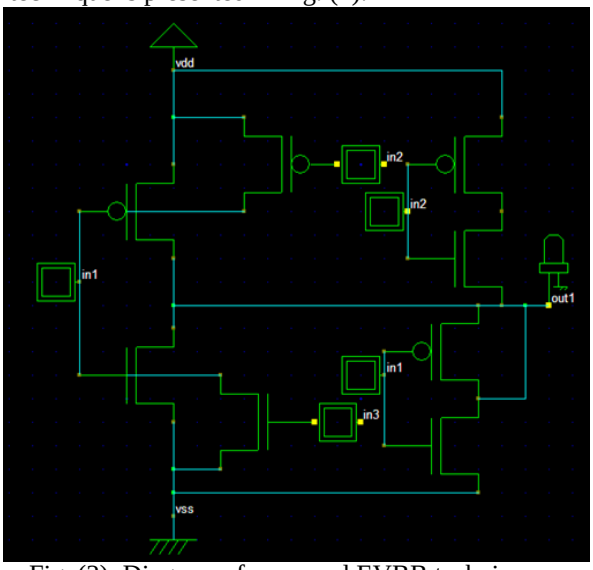

Fig. (2): Diagram of proposed EVBB technique

This proposed method is called body biasing method because sleep PMOS transistor source V_{dd} is connected with the body with another sleep PMOS transistor and sleep NMOS transistor drain V_{ss} is connected with the body with another sleep NMOS transistor. Basically, by increasing the threshold voltage to minimize power dissipation of CMOS circuits, body biasing with bypass technique has been introduced. In the introduced technique, sleep transistor technique has been incorporated with body biasing technique for making the technique more stable. In proposed technique, bypass method has been incorporated to acquire the authentic state at output as sleep transistor technique is a state destructive technique. Here bypass is used to retain the state of the proposed circuit at output.

IV. METHODOLOGY

In this section an efficient methodology has been introduced to decrease the power leakage in CMOS VLSI circuits. The circuit design and simulation have been done by using MICROWIND software. MICROWIND consist two types of window one is DSCH and another is MICROWIND. All the schematic diagram is designed by using DSCH window and the layout or the simulation results have been done by using MICROWIND window. All the parameter of the proposed circuit is estimated by using MICROWIND window where are layouts are designed.

In DSCH all the schematic diagram is designed, and schematic diagram is converted into Verilog file. In MICROWIND window the Verilog files are compiled. The layout of the circuit diagrams is generated after compilation of Verilog files and all the layout diagrams are designed in MICROWIND frame. Subsequently the simulations of all generated layouts have been executed by using Verilog files. From layout design, area of the proposed circuit has been measured and from simulations, leakage power and delay etc. have been measured. Fig. (3) Shows the block diagram of proposed experimental methodology.

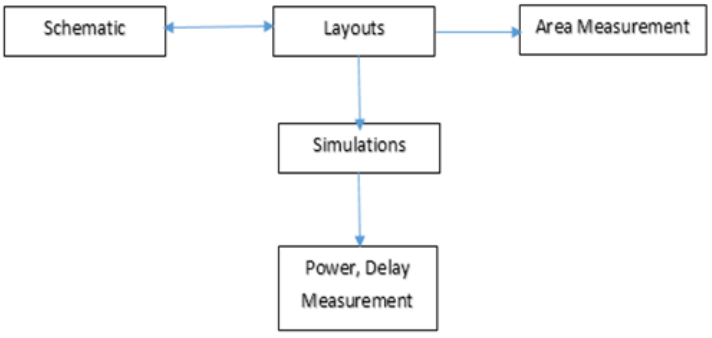

Fig. (3): Experimental Methodology

V. RESULT AND DISCUSSION

In this section the proposed model has simulated in 45 nm technology and all the results are depicted in Fig. (4) to Fig. (6) for measurement of leakage power, delay time and area. The proposed variable body biasing with bypass gives the more significant result as depicted in the below figures.

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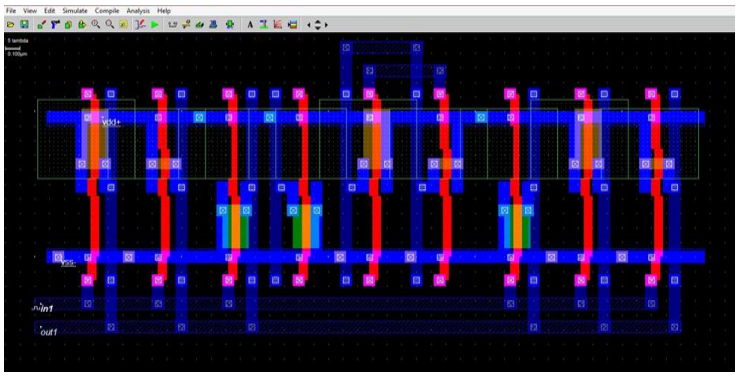

Fig. (4): Layout diagram of efficient variable body biasing with bypass technique

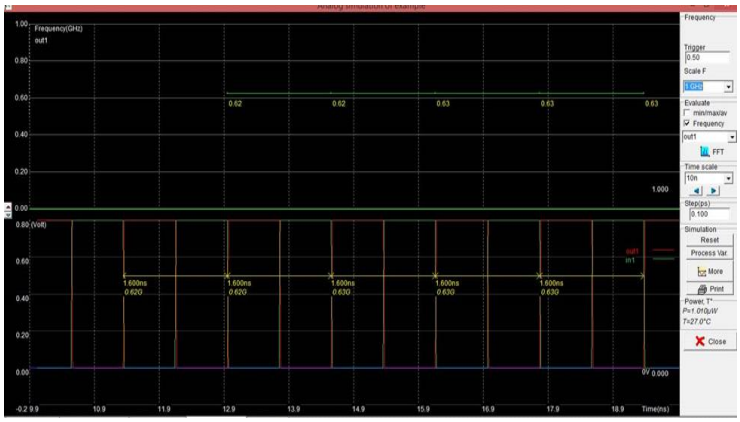

Fig. (5): Frequency vs. time characteristics of efficient variable body biasing with bypass technique

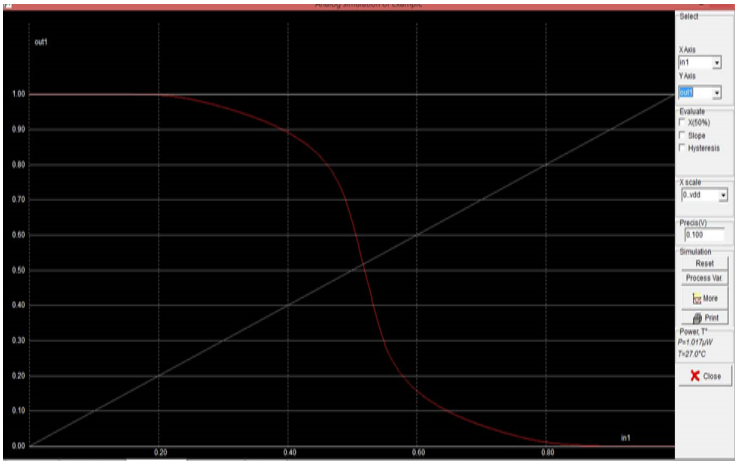

Fig. (6): Voltage vs Voltage characteristics of efficient variable body biasing with bypass technique

The layout area is measured from Fig. (4) and the power dissipation is measured from Fig. (5). From Fig. (6), the voltage of the proposed approach has been measured. It is concluded from the figure that the performance of the proposed EVBB method is more efficient than the existing standard leakage power reduction method. It is shown in figure that the proposed approach has less delay and it deliver maximum current than the existing technique and the proposed technique reduces maximum leakage power as shown in figure.

Simulations result of proposed EVBB technique is compared with the previous leakage power reduction technique in terms of leakage power, area and time delay. Also, it is determined from the experimental table that the proposed EVBB technique has less delay, minimum leakage power and required less area for implementation. So, it is revealed that, there is significant improvement of the proposed scheme in terms of leakage power, area of CMOS circuit and time delay.

TABLE: COMPARISON TABLE BETWEEN FORCED STACK, SLEEP TRANSISTOR, SLEEPY KEEPER, SLEEPY STACK AND PROPOSED

Techniques	**Parameters**		
	Leakage power (µw)	**Time delay (ns)**	**Area of CMOS circuit ($µm^2$)**
Forced Stack	8.876	20	28.50
Sleep Transistor	2.747	4.5	33.06
Sleepy keeper	5.514	41.5	50.22
Sleepy Stack	6.014	9	50.22
Efficient Variable Body Biasing with Bypass (EVBB)	1.017	1.62	6.6776

From table, it is concluded that the proposed EVBB technique gives more significant result than the previous existing leakage power reduction technique. The propped EVBB technique requires less area and the time delay of the proposed technique is minimum than the existing technique. The proposed EVBB technique gives faster response than the previous technique. It is also found out from the table that proposed EVBB technique reduces maximum leakage power.

VI. CONCLUSION

Power leakage is one of the serious concerns in nanometer in CMOS technology. As the technology has been advances day by day and the requirement of battery-operated device demand increases exponentially, so low power, high performance digital CMOS technology has been projected in this work. An efficient technique has been introduced in this paper to decrease the power leakage in CMOS circuits. It can observed from the simulation of the proposed technique that the proposed EVBB technique gives more significant result in terms of ultra-low static power consumption with state saving and it is observed from the result that the proposed EVBB technique is more efficient technique than the other leakage reduction technique.

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