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Design of FPGA-based Digital PID Controller Using Xilinx SysGen® For Regulating Blood Glucose Level of Type-I Diabetic Patients

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Abstract

This paper emphasizes on a method for designing digital PID controller based on Field Programmable Gate Array (FPGA) device for regulating blood glucose level of type-I diabetic patients. The controller is tuned using Bergman Minimal model as a diabetic patient model in MATLAB and Simulink environment. The PID parameters are tuned using a genetic algorithm (GA). Because the speed of control systems has influence on their performance and stability, Field Programmable Gate Array (FPGA) device is considered. A Simulink to FPGA flow is applied to the structure of PID controller with Xilinx blocks in Simulink. The results of blood glucose of two diabetic patient models using different quantization in bits are simulated. The results show that unsuitable number of bits cause hypoglycemia and increasing the peak of blood glucose in diabetic patients. System Generator and Integrated Software Environment (ISE) are used for creating Bitstream file that can be downloaded into FPGA device. The results show that implementation of PID controller on FPGA using System Generator is compact and high speed and causes the designer can evaluate and implement different designs simply.

Keywords: Digital PID controller, type-I diabetic patients, blood glucose, FPGA, Xilinx ISE design suite, System Generator, MATLAB/Simulink.

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1. Introduction

Diabetes mellitus is a metabolic disease in which the body does not produce or properly use insulin. The pancreatic hormones insulin and glucagon which are secreted from β-cells and α-cells respectively are responsible for keeping the blood glucose concentration level in a normal range [1, 2]. There are two types of diabetes: type I and type II. Type-I diabetes mellitus (TIDM) is a disease characterized by absence or death of the β-cells in the pancreatic islets of Langerhans. High average glucose concentration (above 7mmol/l) is called Hyperglycemia [3]. Hypoglycemia is a complication that occurs for TIDM when the blood glucose level is too low (less than 2 mmol/L [4]). Since the β-cells are responsible to produce insulin, external insulin injections in TIDM are required to regulate the blood glucose concentration.

Blood glucose control of diabetics can be categorized to open-loop and closed-loop systems. Typical diabetic treatment is based on open-loop control in which patient measures own blood glucose 3 or 4 times in a day and try to regulate it in a normal range by injecting appropriate dose of insulin. This method is not accurate because of time duration between the measurements. In closed-loop control systems, sensor measures blood glucose of diabetic patient periodically and sends this information to the controller. Then the controller demonstrates appropriate dose of insulin. The object of designing controller is shown in Table 1.

Multiply and accumulate are two operations that used in most of the control computations. When any kind of digital controller is doing these operations, the computational overhead will reach its maximum. So the sampling rate and speed are limited by the rate at which the system performs these operations. Because the speed of control system has influence on its performance, stability, robustness and disturbance rejection characteristics, FPGAs are good choice. Speed of FPGAs is very fast and the

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control loop rate only is limited by the sensors, actuators and I/O modules [5]. Also features such as non-interrupt-driven, parallel processing of data and configurable word widths, makes FPGAs a good choice for implementation of digital controllers [6]. System Generator is a system-level modeling tool that simplifies FPGA hardware design. By using this tool the designer with a little knowledge about FPGA hardware and Hardware Description Language (HDL) can develops Simulink in many ways to provide a modeling environment that is appropriated to hardware design [7]. FPGA based designs have been used in digital systems by many researchers. Murthy et al. in 2008 implement a Simulink model of an Unmanned Ground Vehicle (UGV) based on RC-Truck on FPGA using system generator. The control system consisted of a simple mission planner to generate a vector of waypoints, a PI velocity controller and a proportional heading controller [8]. Alvis et al. discussed FPGA based flexible autopilot platform for unmanned systems [9].

Kalage et al. offered simulation of FPGA based direct torque control of induction motor drive using system generator [10]. Gupta et al. in 2010 designed and implemented a PID controller for controlling the speed of DC motor on FPGA using system generator [11]. Many controllers for regulating blood glucose level were proposed. Most of them were based on PID controller [12-17]. The results of Steil et al. in 2004 showed that this controller "closely parallels the β-cell biphasic insulin response" [12]. In this study we designed and simulated a PID controller for regulating blood glucose of type-I diabetic patients based on FPGA using Xilinx system generator. In section 2 the physiological model of glucose-insulin regulatory system in TIDM is introduced. Section 3 includes the design of PID controller using Xilinx system generator. The features that are important in design flow with system generator are discussed in this section. In section 4 simulation results of designed PID controller is done. Finally, the paper is finished with the interpretation and discussion of the results.

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Table 1. Control objective of glucose-insulin system [18]

Glucose (mg/dl)	Normal	Target
Before eating	<110	90< <130
Two hours after eating	<110	<180
Bed time	<120	110< <150

2. Glucose-Insulin System Model

Although complicated models are accurate to describe glucose-insulin metabolism, but in many cases a simple model would be sufficient to make a good analysis. A simple method with few parameters was introduced by Richard N. Bergman and is called Bergman's minimal model. The model equations are [19]:

$$\begin{aligned}\frac{dG(t)}{dt} &= p_1[G(t) - G_b] - X(t)G(t) + D(t)\\ \frac{dX(t)}{dt} &= -p_2 X(t) + p_3[I(t) - I_b]\\ \frac{dI(t)}{dt} &= -n[I(t) - I_b] + \gamma[G(t) - h]^{+} t + U(t)\end{aligned} \quad (1)$$

Where $G(t)$ is the plasma glucose concentration over basal (mg/dl), G_b is the basal plasma glucose (mg/dl), $X(t)$ is the effect of active insulin (1/min), $I(t)$ is the insulin concentration above basal (mU/L), I_b is the basal insulin level (mU/L), $D(t)$ is the rate of mg glucose pr. dL entering the blood. $U(t)$ is the external insulin input (mU/L/min). p_1, p_2, p_3, n, h and γ are parameters of Bergman minimal model. γ is rate of pancreatic release of insulin after glucose bolus [(mU/L) $(min)^{-1}$ $(mg/dl)^{-1}$]. n is decay rate of blood

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insulin (1/min), and h is the threshold value of blood glucose above which pancreatic β-cells release insulin (mg/dl). The term $\gamma[G(t)-h]^+$ demonstrates insulin secretion in the body which does not exist in TIDM. The clinical data express that the value of p_1 parameter in diabetic patients reduced extremely and can be approximated to zero.

A simple description of $D(t)$ was suggested by Fisher and looks like "Equation (2)" [20]:

$$D(t) = B\exp(-\alpha t) \qquad B > 0 \tag{2}$$

3. Design of PID Controller

One of the frequently used controllers is the PID controller. The controller equation is:

$$u(t) = k_p e(t) + k_d \frac{de(t)}{dt} + k_I \int_0^t e(a)da \tag{3}$$

Where k_p is proportional gain, k_d is derivative gain, k_I is integral gain, $e(t)$ is difference between setpoint and blood glucose and $u(t)$ is output of the controller. To obtain the pulse transfer function of digital PID controller, we should discretize "Equation (3)". The result is:

$$U(z) = [k_p + \frac{k_d}{T}(1-z^{-1}) + \frac{k_I T}{2}(\frac{1+z^{-1}}{1-z^{-1}})]E(z) \tag{4}$$

Where T is sampling period.

3.1. Tuning of PID Controller

The parameters of this controller are tuned based on Genetic Algorithm. Genetic Algorithms (GA's) are a stochastic global search method that mimics the natural evolution

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process [21, 22]. The population of a genetic algorithm is demonstrated by a real-valued number or a binary string called a chromosome. How well an individual performs a task is measured by the goal function. The goal function assigns each individual a corresponding number called its fitness. The fitness of each chromosome is assessed and a survival of the fittest strategy is applied [23]. There are three main stages of a genetic algorithm known as reproduction, crossover and mutation.

3.1.1. Reproduction

During the reproduction phase, best chromosomes from latest generation can combine with each other and leave offspring. In our algorithm two best chromosomes from last generation would remain unchanged among new chromosomes in order to achieve faster optimization.

3.1.2. Crossover

Once the selection process is completed, the crossover algorithm is initiated. The crossover probability represents how often crossover is performed. A probability of 0% means that the 'offspring' will be exact replicas of their 'parents' and a probability of 100% means that each generation will be composed of entirely new offspring [23]. Crossover probability in this algorithm was 86%.

3.1.3. Mutation

Although selection and crossover will generate a large amount of different strings, bad choice of initial population will cause the Genetic Algorithm converge on suboptimum strings. This problem may be overcome by a mutation operator into the Genetic Algorithm. In this algorithm we used mutation probability of 1.8%.

The PID parameters are: $k_p = 7, k_d = 140, k_I = 0.005$

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3.2. Designing Controller

The System Generator is a Xilinx toolbox in Simulink environment that can generate HDL code of designs in Simulink automatically. At first the model of PID controller is depicted in Simulink environment for tuning the parameters and evaluation output results of controller. After verifying the performance, the block diagram of controller is drawn again using equivalent Xilinx blocks that are supported in Simulink environment. In these blocks the size of quantization of inputs is determined by *Gateway in* blocks. Also the output size of each computational block including of *AddSub* and *Mult* blocks is determined. After evaluating the results, the HDL code can be generated using system generator block. In this block, we determine the type of FPGA device, the type of generated code (Verilog or VHDL), the FPGA clock period and other desired features. After this step, we continue the process using ISE software. The block diagram of PID controller using Xilinx blocks is shown in figure 1.

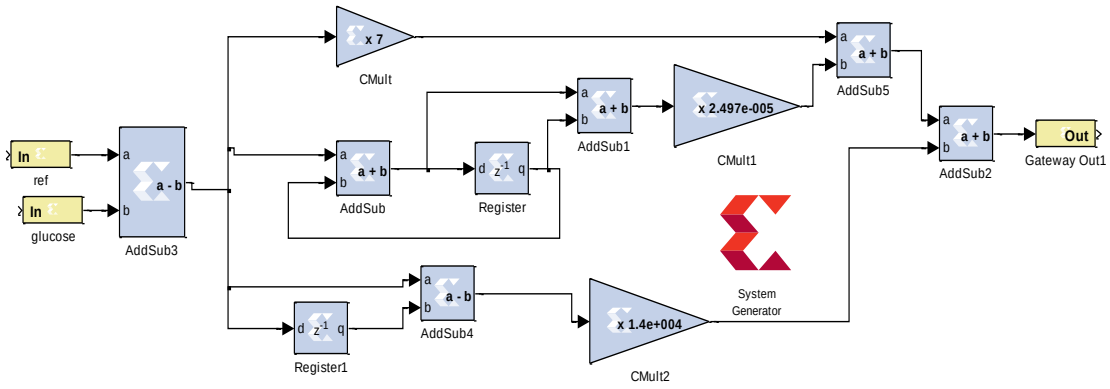

Figure 1. Block diagram of digital PID controller using Xilinx blocks in Simulink environment.

There are several timing values that should be determined in process of design with system generator include of FPGA clock period, Simulink system period and sample period. FPGA clock period specifies the main clock input to the FPGA form which other

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clock and clock enables are derived and so its value only affects to hardware. The Simulink system period establishes a global link between simulation and hardware. This value specifies in the simulation process how often the system generator blocks are summoned [6]. The sample period explains during the simulation how many times the call will block. These should arrive before the block mutates its state. This value can be determined in Gateway in block by the designer [24]. By using block parameters in Xilinx blocks, we control the word widths of different signals. After verifying the timing values, blood glucose level of each patient is simulated using different number of bits of Xilinx block. We consider two sets of bits for signals according to Table 2. This capability of system generator, enables we to control the widths of bits (and so the hardware utilization) and evaluate our design. The results of two states are simulated for each diabetic patient. After evaluation of results, we use System Generator for generating VHDL code. In System Generator toolbox, we use XC3S400-5PQ208 in Xilinx family. The results of hardware utilization using two states according to Table 2, are shown in Table 3.

Table 2. The number of bits that considered for each Xilinx block

Number of bits	Type of Xilinx Blocks										
	Gateway in (ref)	Gateway in (glucose)	CMult	CMult1	CMult2	AddSub	AddSub1	AddSub2	AddSub3	AddSub4	AddSub5
State 1	8	8	12	12	24	8	9	10	8	8	24
State 2	16	16	20	20	32	16	17	16	16	16	32

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Results

In this section, using the designed controller, the simulation results of blood glucose of two diabetic patient models are presented and discussed. The values of patient parameters are in [19]. Blood glucose of each diabetic patient is simulated by using two ways (PID controller block in Simulink and PID controller using Xilinx blocks in Simulink). It was assumed that two patients began to eat meal after a long time (8 hours) after using the controller.

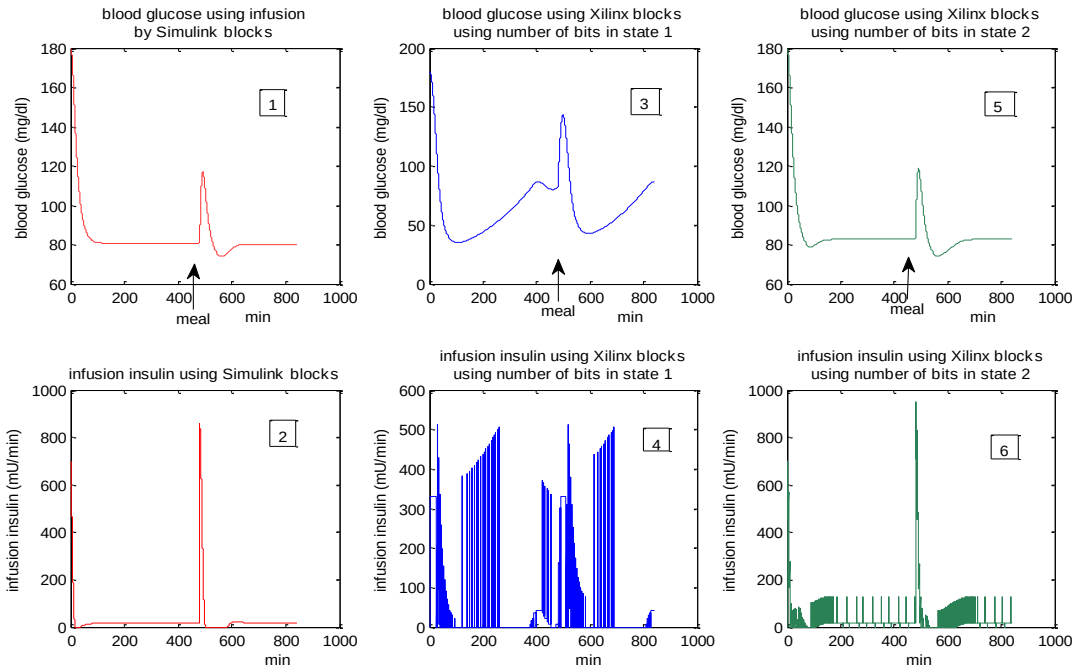

Figure 2. Results of patient 1. Number (1) and (2) show blood glucose and infusion of insulin in patient 1 respectively using Simulink blocks in S domain. Number (3) and number (4) show blood glucose and infusion of insulin in patient 1 respectively using Xilinx blocks in state 1 according to Table 2. Number (5) and number (6) show blood glucose and infusion of insulin in patient 1 respectively using Xilinx blocks in state 2 according to Table 2.

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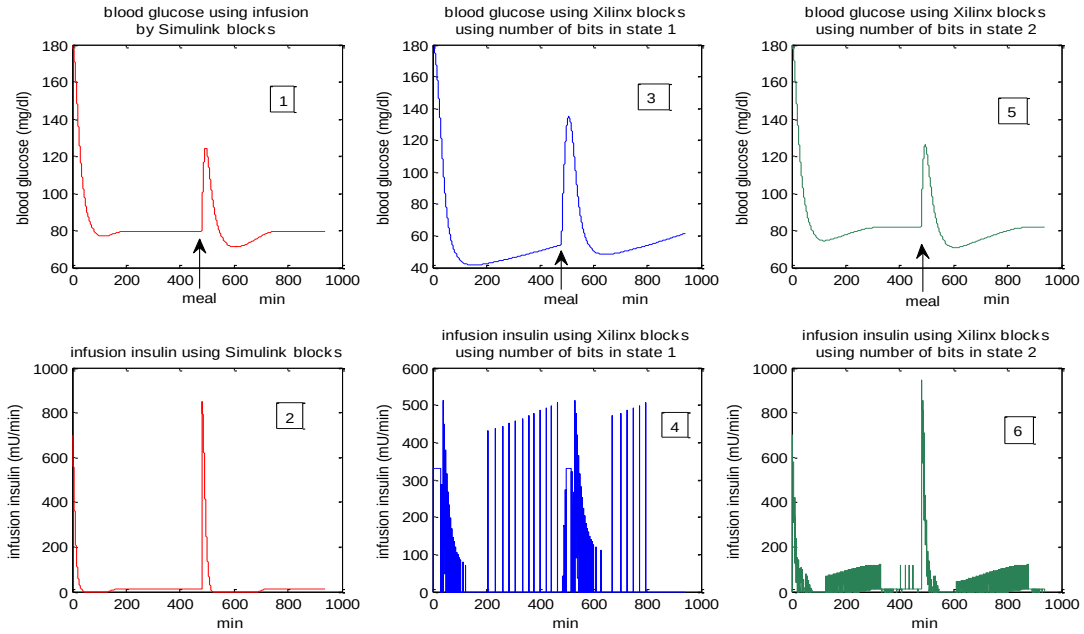

Figure 3. Results of patient 2. Number (1) and (2) show blood glucose and infusion of insulin in patient 2 respectively using Simulink blocks in S domain. Number (3) and number (4) show blood glucose and infusion of insulin in patient 2 respectively using Xilinx blocks in state 1 according to Table 2. Number (5) and number (6) show blood glucose and infusion of insulin in patient 2 respectively using Xilinx blocks in state 2 according to Table 2.

Table 3. Design summery of designing digital PID controller in state 1 and state 2 (according to Table 2) using Xilinx system generator in ISE environment using XC3S400-5PQ208.

Logic Utilization	Used		Available	Utilization	
	State 1	State 2		State 1	State 2
Number of slices flip flops	13	41	3840	1%	1%
Number of 4 inputs LUTs	78	319	3840	2%	8%
Number of occupied Slices	44	185	1920	2%	9%

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Number of Slices containing only related logic	44	185	44	100%	100%
Number of Slices containing unrelated logic	0	0	44	0%	0%
Total Number of 4 input LUTs	82	*353*	3840	2%	*9%*
Number used as logic	78	*319*			
Number used as a route-thru	4	34			
Number of bonded IOBs	25	41	141	17%	29%
Number of BUFGMUXs	1	1	8	12%	12%
Average Fanout of Non-Clock Nets	1.94	1.99			

Table 4. Design summery of designing digital PID controller for diabetic patients using Xilinx blocks.

Patient Number	**Blood Glucose (mg/dl)**			
	Two hours after eating		**Average blood glucose (before eating and bedtime)**	
	State 1	**State 2**	**State 1**	**State 2**
Patient 1	43	77	83	82
Patient 2	46	71	63	82

Discussion

In this study a digital PID controller for maintaining the blood glucose level of type-I diabetic patients in a normal range, has been designed. Performance of this controller was tested by two groups of diabetic patient models with different parameters and different weights in presence of exogenous glucose meal.

In simulation process, after verifying the performance of PID controller in S domain, the block diagram of controller was drawn again using equivalent Xilinx blocks that are

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supported in Simulink environment. In these blocks, timing values and number of bits for each block are chosen. In this work we consider how mathematical model of PID controller that verified in Simulink environment, are implemented between Simulink and the logic based hardware. By using this graphical environment, the need of a detailed knowledge of HDL is no longer required.

Also this method reduces the time required to implement the control design. Utilizing the System Generator allows the designer to consider the design options in terms of size and speed to perform the design constraints. There are several parameters such as timing values and number of bits of each Xilinx block that should be considered in process of design. For indicating the effect of number of bits, we consider two states with different number of bits (Table 2). In state 1, number of bits was lower than state 2. The blood glucose of each diabetic patient model is simulated using these two states.

The simulation results show that the peak of blood glucose in two patients in state 1 was higher than state 2. Also according to simulation results, using the number of bits in state 1, led to hypoglycaemia in two patients. But using the number of bits in state 2, could regulate blood glucose of two patients well. The HDL of PID controller in two states was generated automatically using system generator tool. Synthesize, implementation and generate programming file was done in ISE environment. Table 3 shows the hardware utilization of designed digital PID controller in two states.

As it is seen, hardware utilization of state 2 is larger than state 1. But The results show that implementing of PID controller using system generator on FPGA is very power efficient, compact and high speed in either two states.

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