

A Comparative Study on Two different Flyback Configurations at Input PFC Stage for Lighting Applications

Anjali R.N¹ and K.Shanmukha Sundar²

¹Dept. of EEE, Dayananda Sagar College of Engineering, Bangalore, Karnataka, India

²Prof. and Head, Dept. of EEE, Dayananda Sagar College of Engineering, Bangalore, Karnataka, India

*Corresponding Author's E-mail: anju.ratehalli@gmail.com

Abstract

Two different Flyback configuration at input PFC stage for lighting applications are presented in this paper. In both the converter configurations, the input PFC stage consists of two flyback converters with different polarity in order to avoid the input diode bridge rectifier. The design of the converters for 30 W light emitting diode applications is presented. The two converters are simulated using SIMULINK and simulation results are presented in the paper. A comparison in terms of losses and efficiency is carried out between the two converter configurations. A RCD snubber circuit is introduced in the input flyback stage of both the converter configurations to reduce the voltage stress across the switches due to leakage inductance at the primary side of the transformer. The output stage is boost converter circuit.

Keywords: Flyback converters, Electronic ballasts, Power factor correction (PFC).

I. Introduction

Electronic ballast is a device which is used to control the starting voltage and operating currents of lighting device. The electronic ballast for LED lighting applications has received great attention in recent years due to their small size, light weight, long lamp life and higher efficiency in comparison with the traditional electromagnetic ballast. The block diagram of different stages of electronic ballasts for lighting systems presented in this paper is shown in Fig 1.

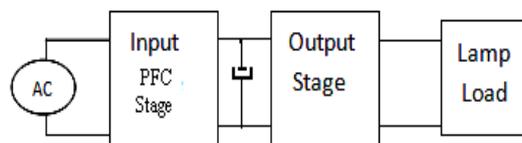


Figure 1: Block diagram of different stages of electronic ballast for lighting systems

The input PFC stage is the integration of two flyback converters, one for each polarity of line voltage. The input PFC stage supplies a capacitor which provides constant voltage across the output stage. The output stage is the boost converter circuit which is used to obtain desired voltage required to supply LED lighting systems. In the literature, electronic ballasts used diode bridge rectifier followed by boost converter as the input PFC stage due to its simplicity and good power factor performance. The diode bridge rectifier causes voltage drop and lowers the efficiency of the overall system. Therefore, if the diode bridge rectifier is eliminated, the efficiency of the converter is increased. The flyback converter is buck-boost converter with transformer isolation. The transformer

of the flyback transformer is not a normal transformer, as its function is to store energy when the switch is ON and deliver the stored energy to load when the switch is OFF. The transformer is similar to storage inductor with primary and secondary winding.

II. Input PFC Stage

In this section, the input PFC stage of two different converter configurations is presented. The input PFC stage for both the converter configurations consists of two flyback converters with different polarity in order to avoid diode bridge rectifier. Here, the discontinuous conduction mode (DCM) of the flyback stage is considered.

i. Input PFC stage of Converter configuration 1[1]

The circuit topology is shown in Fig 2. It consists of two MOSFETs connected in the primary side of the flyback transformer and one MOSFET connected in the secondary side of the transformer. The output capacitor is used to reduce the output voltage ripple.

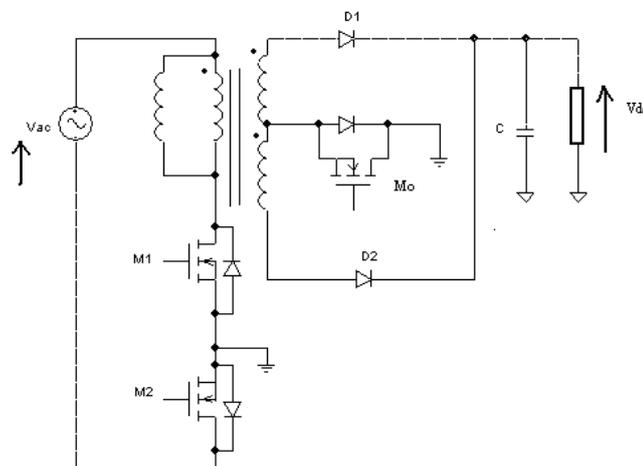


Figure 2: Circuit diagram of input PFC stage of converter configuration 1[1]

A. Operation under positive input voltage

The operation under positive input voltage can be explained in two modes

Mode 1: The Mode 1 operation under positive input voltage is explained with respect to Fig. 3(a). In this mode, switch M_1 is turned ON and M_2 is turned OFF. When switch M_1 turns ON by the gate pulses obtained from the pulse generator, the input line voltage, i.e., V_{AC} is applied to the primary side of the Flyback transformer and the Mosfet as shown in Fig 3(a).

The magnetizing inductance of the transformer begins to charge, the current flowing in the primary winding induces voltage across secondary winding i.e U_{s1} and U_{s2} as shown in Fig 3(a). The diode D_2 is reverse biased, and thus, no current flows through the secondary winding connected to D_2 . On the other hand, D_1 would be conducting with the polarity of the voltage U_{s1} , and thus, the additional output MOSFET M_0 is necessary in order to block that current. Hence, M_0 must be turned OFF during this operation mode.

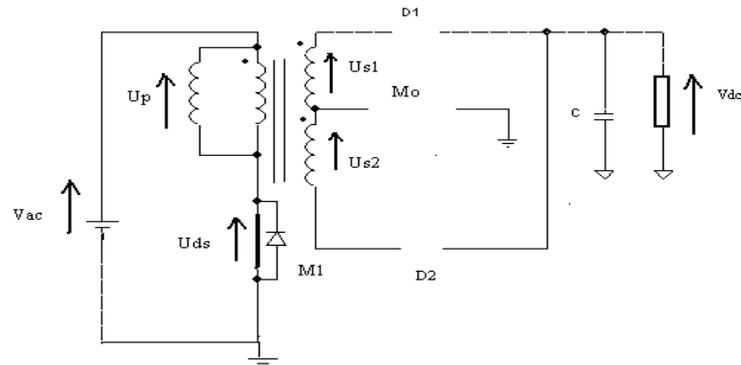


Figure 3(a): Mode 1 of positive input voltage

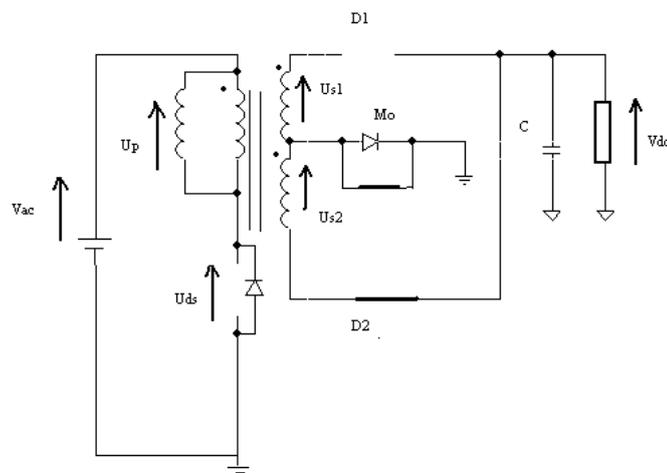


Figure 3(b): Mode 2 of positive input voltage

Mode 2: The Mode 2 operation under positive input voltage is explained with respect to Fig. 3(b). In this mode, both the switches M_1 and M_2 are turned OFF. In this mode, the magnetizing inductance, which is charged during Mode 1, discharges through the secondary side, forward biasing the diode D_2 . The switch M_0 must be turned ON in order to allow this current flowing through D_1 . Once the magnetizing inductor of the transformer is fully demagnetized, diode D_2 results in reverse biased and no current flows through the secondary of the transformer. Once the magnetizing inductor of the transformer is fully demagnetized, diode D_2 results in reverse biased and no current flows through the secondary of the transformer.

B. Operation under negative input voltage

In the circuit diagram shown in Fig 2, there is symmetry in the circuit with respect to the input voltage. The operation under negative input voltage is similar to the operation under positive input voltage, only interchanging the subscripts "1" and "2" in the previous explanation.

ii. Input PFC stage of Converter configuration 2

The circuit diagram is shown in Fig 4. It consists two MOSFETs connected in the primary side of the flyback transformer.

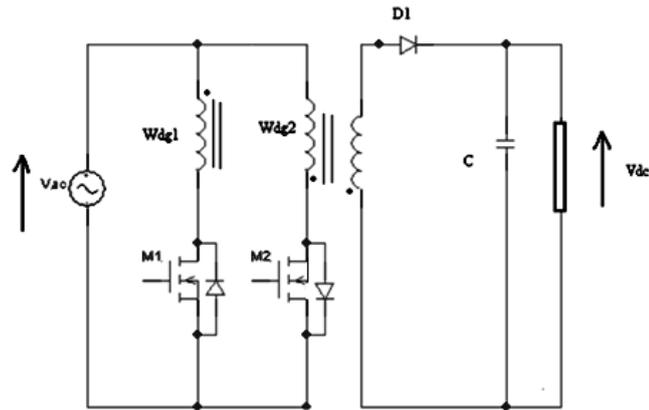


Figure 4: Circuit diagram of input PFC stage of converter configuration 2

A. Operation under positive input voltage

The operation can be explained in two modes

Mode 1: During Mode 1, switch M_1 is turned ON and M_2 is turned OFF. When switch M_1 turns ON, the input line voltage is applied to the primary winding 1 of the transformer as shown in Fig 5(a). The current through the primary winding increases and magnetizing inductance of the transformer begins to charge during this period. From Fig 5(a) the diode D_1 is reverse biased and therefore no current flows through the secondary side of the transformer.

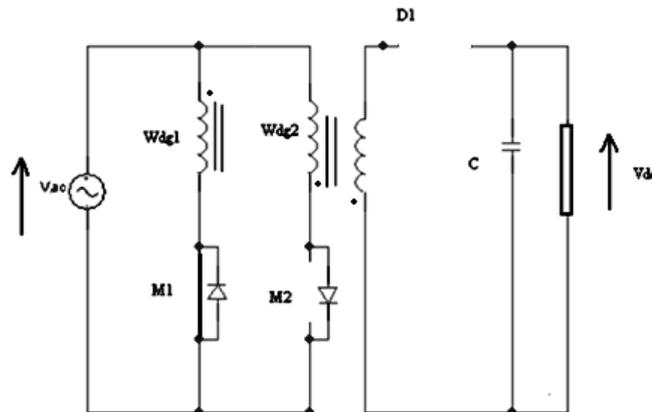


Figure 5: (a) Mode 1 of positive line voltage

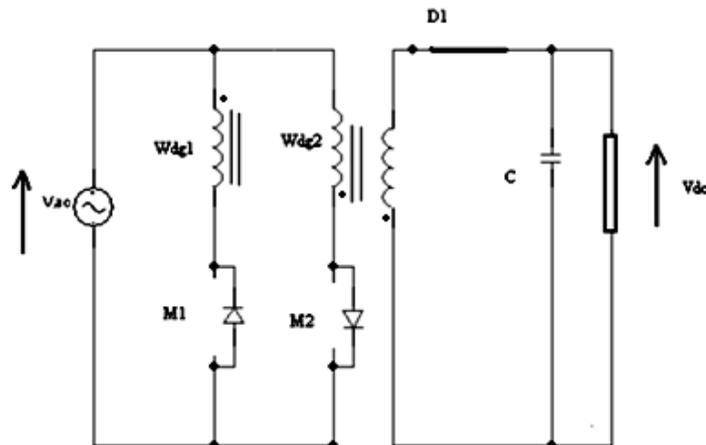


Figure 5: (b) Mode 2 of positive line voltage

Mode 2: During this mode, both the switches M_1 & M_2 are turned off. The magnetizing inductance discharges through the secondary side of the transformer and polarity of the winding reverses. Now the diode D_1 becomes forward biased as shown in the Fig 5(b). The energy stored in the inductor flows through the secondary diode and into the capacitor and the load. Once the magnetizing inductor of the transformer is fully demagnetized, the diode D_1 results in reverse biased and no current flows through the transformer.

B. Operation under negative input voltage

In the circuit diagram shown in Fig 4, there is symmetry in the circuit with respect to input voltage. The operation under negative input voltage is similar to the operation under positive input voltage, except with interchanging of MOSFET M_1 by M_2

III. Design details of the Input PC stage for 30W LED lamp

The target lamp is 30W LED lamp. The design equations for the input stage are

$$\eta_{FLY} = 90\% \quad (1)$$

$$f_{switch} = 100KHz \quad (2)$$

$$V_{ACRMSMAX} = 276 V_{RMS} \quad (3)$$

$$V_{ACRMSMIN} = 92 V_{RMS} \quad (4)$$

$$d_{AC} = 0.5 \quad (5)$$

$$P_{FLY} = \frac{P_{LEDs}}{\eta_{OUT}} = \frac{30}{0.9} = 33W \quad (6)$$

Where η_{FLY} is the estimated efficiency of the flyback stage, f_{switch} is the switching frequency of the flyback stage, V_{ACRMS} is the RMS value of the line input voltage, d_{AC} is the duty ratio of the input flyback stage, P_{FLY} is the power output of the flyback stage, P_{LED} is the load power, η_{OUT} is the output stage efficiency. The magnetizing inductance of the flyback converter can be given as:

$$L_{\mu} \leq \frac{(V_{ACRMSMIN} \sqrt{2})^2 d_{AC}^2 \eta_{FLY}}{4 P_{FLY} f_{switch}} \quad (7)$$

Substituting the values in equation 7,

$$L_{\mu} \leq 250 \mu H$$

The design calculations presented in this section, holds good for both the converter configurations.

IV. Output Stage

The output stage is boost converter circuit. The output stage is same for both the converter configurations presented in this paper. The circuit diagram of the boost converter is shown in Fig 6. The switching frequency considered is 100 kHz. The operation of the boost converter can be explained in two modes.

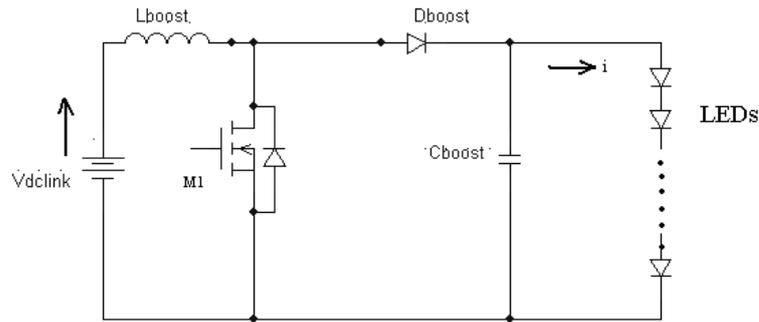


Figure 6: Circuit diagram of output stage (Boost converter) of converter

Mode 1: This mode begins when switch M_1 is turned ON. The voltage across the inductor during this period is V_{dclink} (input voltage). The inductor current rises linearly with a slope of V_{dclink}/L_{boost} . During Mode 1, the current flowing through M_1 is same as the inductor current. The voltage across the diode is V_o (output voltage)

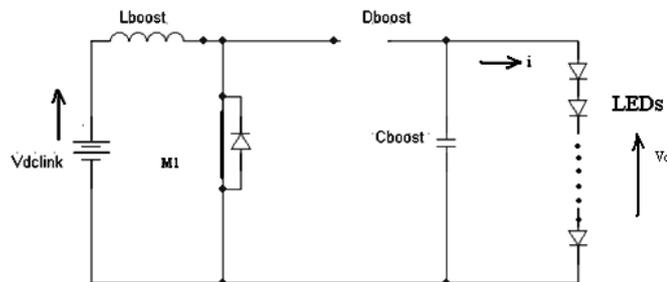


Figure 7: (a) Mode 1 of positive line voltage

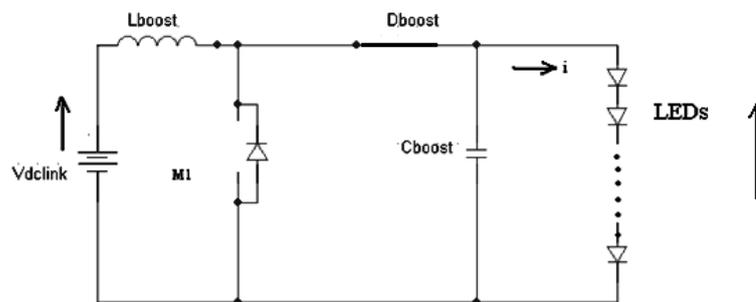


Figure 7: (b) Mode 2 of positive line voltage

Mode 2: The Mode 2 of boost converter is explained using Fig 7(b). During this mode, switch M_1 is turned OFF. The voltage across the inductor is $(V_{dclink} - V_o)$. The inductor current falls linearly with a slope of $(V_{dclink} - V_o) / L_{boost}$. The current flowing through diode is same as the current flowing through the inductor.

Input voltage $V_{IN} = 60V$

Required output voltage $V = 120V$

For Boost converter,

$$\frac{V_o}{V_{IN}} = \frac{1}{1-D} \quad (8)$$

By substituting the values of V_o and V_{IN} , the duty ratio of the boost converter is 0.5

$$\text{Target power output of the boost converter } W = 30 \text{ watts} \quad (9)$$

$$\text{Output current of the boost converter } I_{OUT} = W/V_O = \frac{30}{120} = 250 \text{ mA} \quad (10)$$

$$\text{Load resistance of the boost converter } R = (V_O/I_{OUT}) = 480\Omega \quad (11)$$

$$\text{The value of boost inductor, } L_{boost} \geq \frac{D(1-D)^2XR}{2f} \geq 300\mu\text{H} \quad (12)$$

The value of the boost capacitor is calculated considering 10% output ripple voltage

$$C_{boost} \geq \frac{D}{RXf (\Delta V_O/V_O)} \geq 104\text{nF} \quad (13)$$

Where R is the load resistance and f is the switching frequency of the boost converter.

V. Voltage Snubber

In the operation of the flyback converter, there is a danger of exceeding the voltage ratings of the devices during turn-OFF of the switches due to the leakage inductance at the primary side of the transformer. Therefore, it becomes essential to limit the voltage spikes across the device such that the voltage is within the rating of the device. Various snubber circuits are used in order to reduce the device transient stress. The RCD snubber circuit connected at the input PFC stage of converter 1 configuration [1] is shown in Fig.8

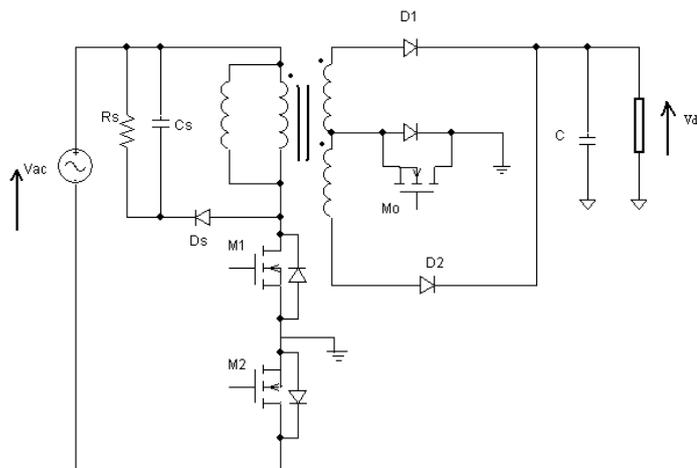


Figure 8: RCD clamp circuit connected at input PFC stage of converter configuration 1 [1]

The RCD snubber is connected across the primary winding of the flyback transformer as shown in the Fig.8. The snubber circuit reduces the voltage stress across the two Mosfets connected in the primary side of the flyback transformer. The RCD snubber circuit connected at the input PFC stage of converter configuration 2 is shown in Fig.9

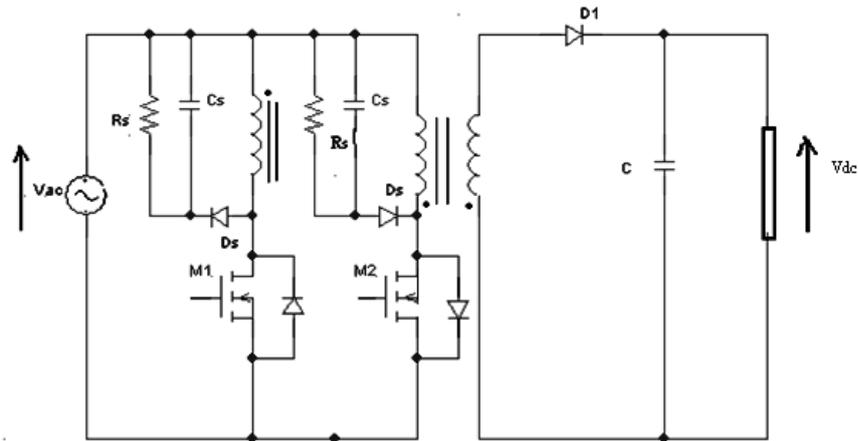


Figure 9: RCD clamp circuit connected at input PFC stage of converter configuration 2

The RCD clamp circuit is connected in both the primary windings of the Flyback transformer as shown in the Fig.9.

VI. SIMULATION RESULTS OF THE CONVERTERS

A. Simulation results of the input stage of converter configuration 1[1]

The simulation has been carried out using MATLAB and the SIMULINK model of the input stage of converter 1 is shown in Fig 10.

Discrete,
Ts = 5e-06 s.
powergui

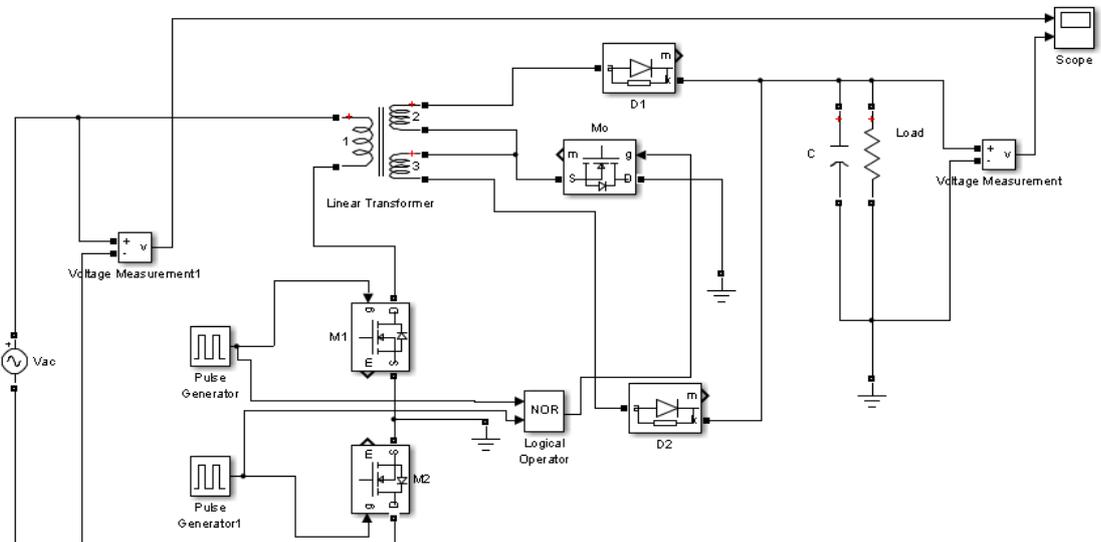


Figure 10: SIMULINK model of input PFC stage of converter configuration 1

The gate pulses required to turn ON the MOSFET is obtained using pulse generator as shown in Fig.10. MOSFET M_1 is turned ON during positive cycle of applied voltage; MOSFET M_2 is turned ON during negative cycle of applied voltage. The MOSFET M_0 is turned ON only when both the MOSFETs M_1 and M_2 are OFF. This can be achieved by using a logical operator NOR, where the two inputs to the NOR operator are from the pulse generators used to turn ON the MOSFETs M_1 and M_2 and the output of NOR operator is given to the gate terminal of MOSFET M_0 . The output voltage and current waveform of the input PFC stage of converter 1 is shown in Fig. 11 (a) and 11(b) respectively.

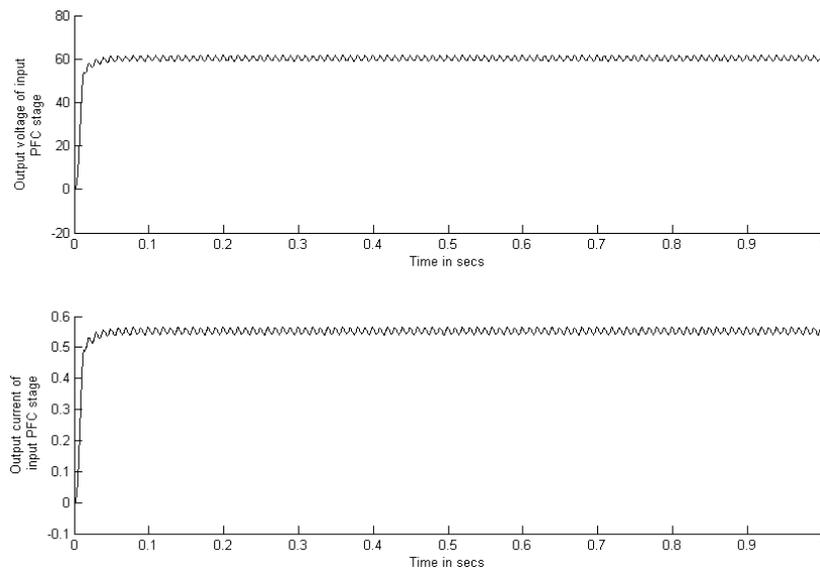


Figure 11: Simulation results of input PFC stage of converter 1

For the 30w LED applications, the required magnitude of voltage at input PFC stage is 60V and the same is obtained at the load terminals of the input flyback stage as shown in Fig 11(a). Further, from Fig 11(d) , it is clear that the output current of 0.55 A is obtained in order to get the desired output power of flyback stage i.e 33W.

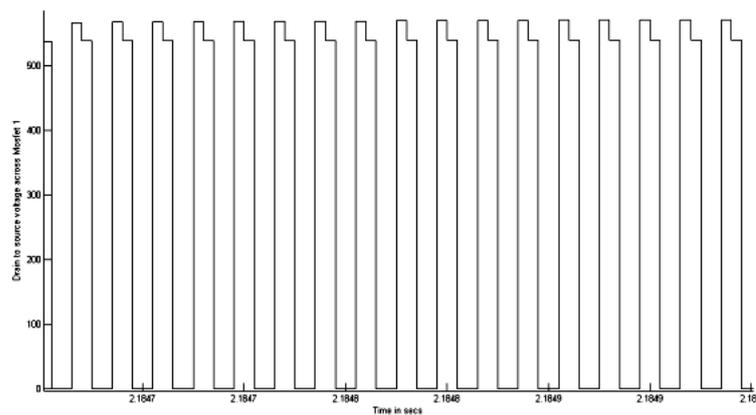


Figure 12: (a) Voltage across the MOSFET M_1 without snubber

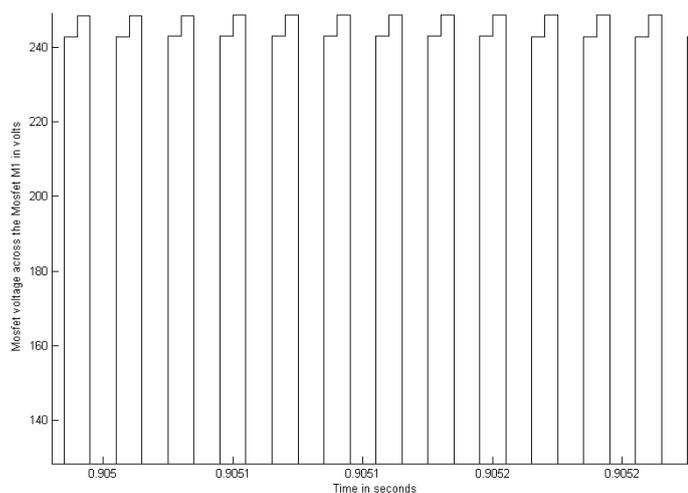


Figure 12: (b) Voltage across the MOSFET M_1 with snubber

Fig 12 (a) shows the voltage across the MOSFET M_1 without snubber circuit. Ideally, the MOSFET M_1 and M_2 experiences drain-source voltage stress equal to the sum of the input voltage and the voltage induced in the primary winding during the OFF period of the MOSFET. In practice, due to the leakage inductance of the transformer, causes voltage stress in addition to the ideally expected voltage stress. Snubber circuits are used to limit the voltage stress to safe levels within the voltage rating of the Mosfet. Without snubber, the peak value of the voltage across the MOSFET M_1 is nearly 550V. The voltage across the MOSFET M_1 with snubber circuit connected in the primary side of the transformer is shown in Fig 12(b). With snubber, the peak value of the voltage across the MOSFET is nearly 250V. From Fig 12, it is clear that snubber circuits connected at the primary side reduce the voltage stress across the switches.

B. Simulation results of the input stage of converter configuration 2

The SIMULINK model of the input stage of converter 2 is shown in Fig 13.

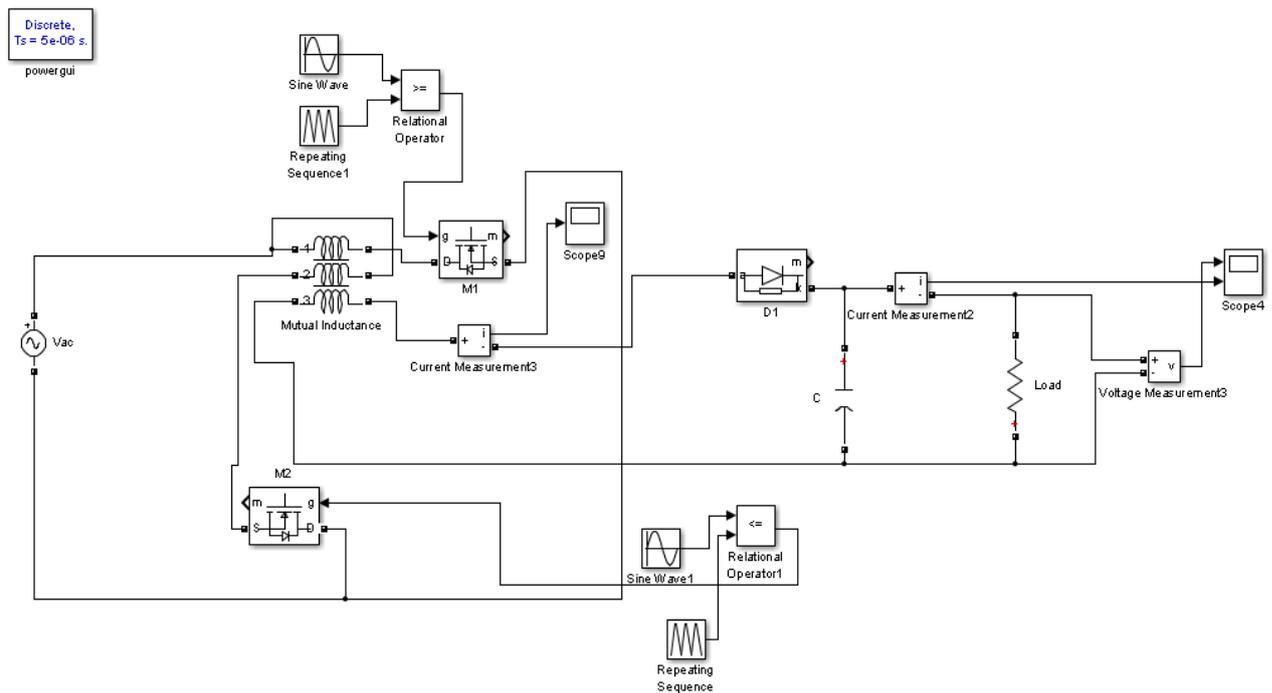


Figure 13: SIMULINK model of input PFC stage of converter 2

The PWM method is used to obtain the gate pulses required to turn ON the MOSFETs M_1 and M_2 alternatively i.e MOSFET M_1 is turned ON during positive half cycle and MOSFET M_2 is turned ON during negative half cycle. The output voltage and current waveforms of the input PFC stage is shown in Fig 14 (a) and (b) respectively.

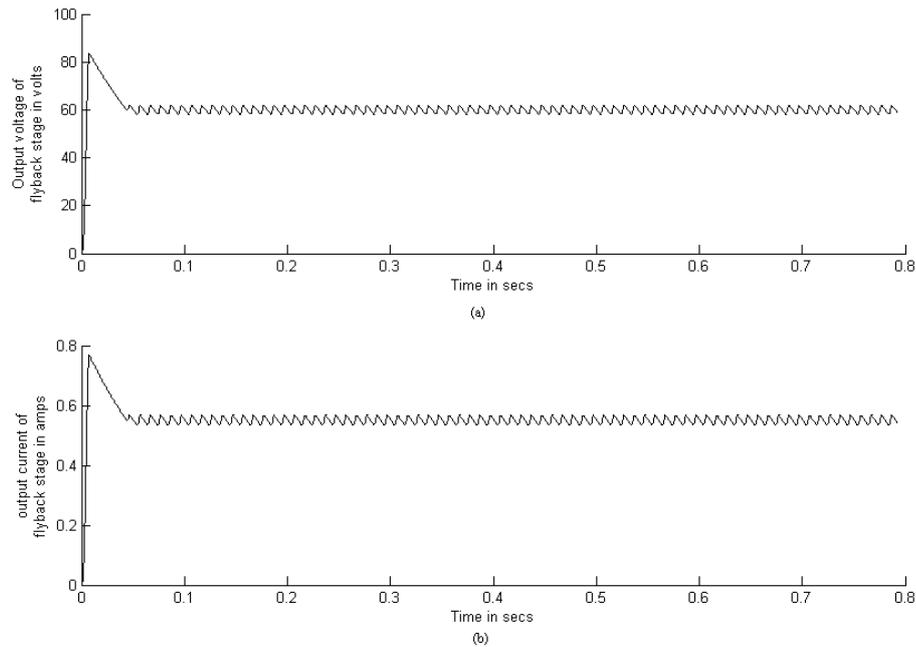


Figure 14: Simulation results of input PFC stage of converter 2

The voltage magnitude of 60V is obtained at the output of the input flyback stage which is desired voltage required for the output stage. The voltage obtained from the flyback stage is applied to the output stage. The output current of 0.55A is obtained as shown in Fig 14(b), in order to get the desired output power.

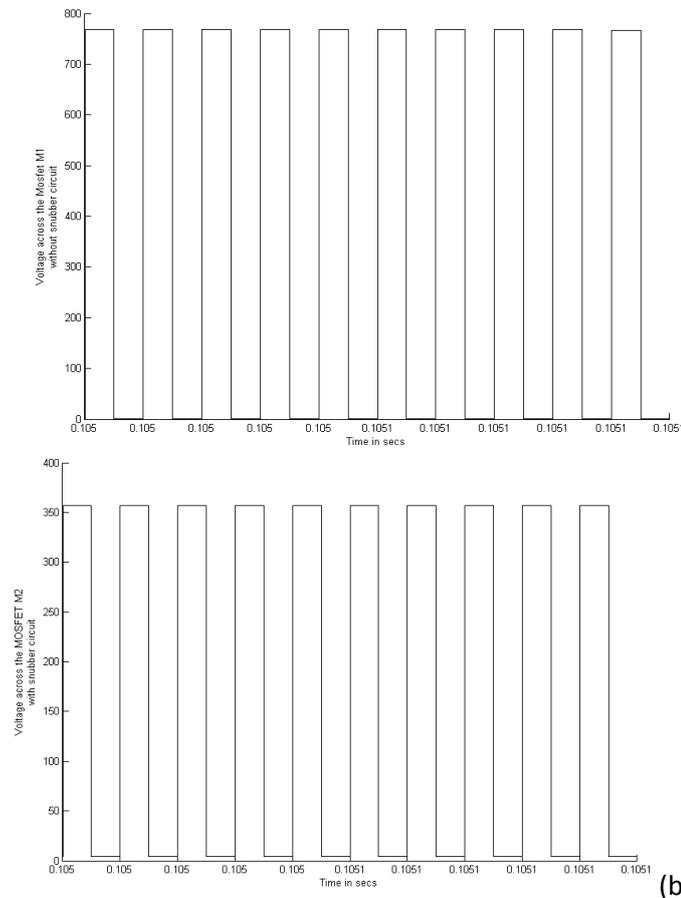


Figure 15: (a) Voltage across the MOSFET M₁ without snubber circuit (b) Voltage across the MOSFET M₁ with snubber circuit

Fig 15(a) shows the drain to source voltage across the MOSFET M_1 when snubber circuit is not connected at the primary side of the transformer. Without the snubber circuit, the peak value of voltage across the MOSFET is nearly 800V as shown in Fig 15(a). This high value of voltage can damage the switches. Hence, the snubber circuit is required to reduce the voltage stress the switches. The drain to source voltage across the MOSFET M_1 with snubber circuit is shown in Fig 15(b). The peak value of voltage across the MOSFET M_1 with snubber circuit is nearly 350V as shown in Fig 15(b).

C. Simulation Results of the output stage

The output voltage of 60 V which is obtained from input flyback stage is applied to the input terminals of the output stage. The SIMULINK model of the output stage (Boost converter) is shown in Fig. 16. The boost converter is needed to step up the voltage from 60V to 120V. An output capacitor is used to reduce the ripple in the output voltage. The output voltage waveform of the Boost converter is shown in Fig.17. From Fig. 17, it is observed that the input voltage 60V is increased to 120V which is desired voltage required to supply LED lighting system. The output stage is same for both the converter configurations presented in this paper.

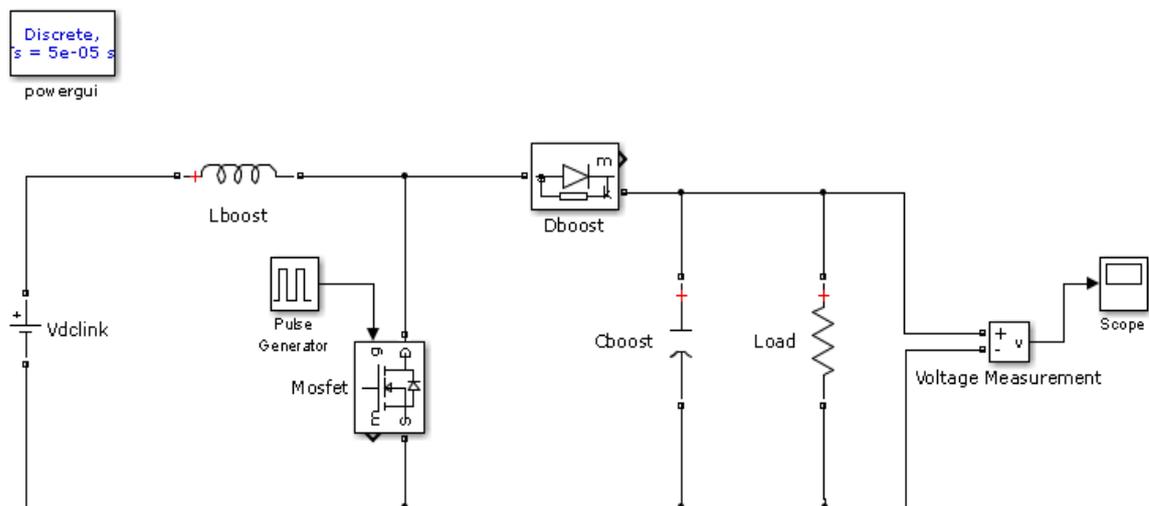


Figure 16: SIMULINK Model of the Output stage

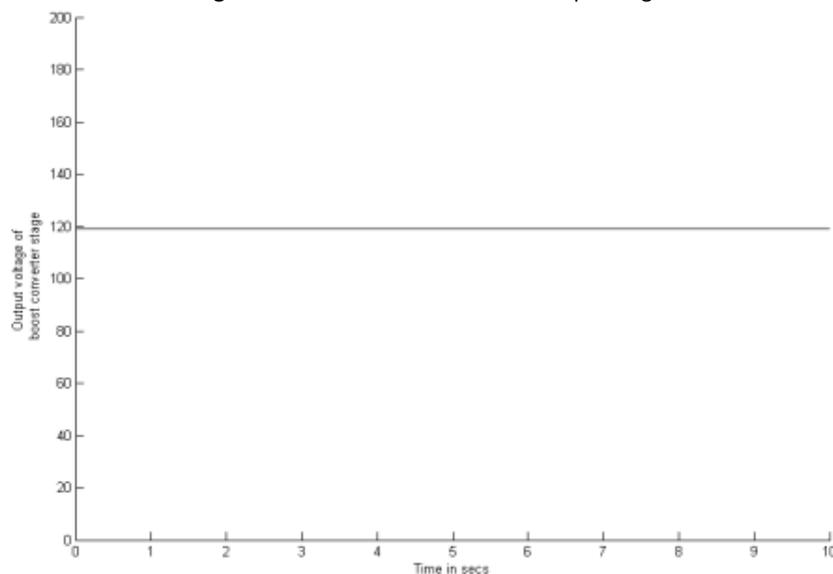


Figure 17: Simulation result of the Output stage

VII. Losses and Efficiency of the Converters

The conduction and switching losses of the various components of both the converters are calculated using simulation results and are depicted in Table I and II.

Table I: Losses in various components of converter 1

Description	Related Equations	Value
Conduction losses in diode D_1 of flyback stage for $I_d = 1.7A$, $R_{don} = 0.001\Omega$	$I_d^2 R_{don}$	2.89 mW
Conduction losses in diode D_2 of flyback stage for $I_d = 1.7A$, $R_{don} = 0.001\Omega$	$I_d^2 R_{don}$	2.89 mW
Conduction losses in MOSFET M_0 of flyback stage for $I_d = 1.7A$, $R_{don} = 0.11\Omega$	$I_d^2 R_{don}$	317.9 mW
Conduction losses in secondary winding of flyback transformer S_1 for $I_{S1} = 1.7A$, $R_S = 0.01\Omega$	$I_{S1}^2 R_S$	28.9 mW
Conduction losses in secondary winding of flyback transformer S_2 for $I_{S1} = 1.7A$, $R_S = 0.01\Omega$	$I_{S2}^2 R_S$	28.9 mW
Conduction losses in diode of output boost converter stage for $I_d = 0.2A$, $R_{don} = 0.001\Omega$	$I_d^2 R_{don}$	0.04mW
Conduction losses in MOSFET of output boost converter stage for $I_d = 0.45A$, $R_{don} = 0.11\Omega$	$I_d^2 R_{don}$	22.2 mW
Switching losses in diode D_1 of flyback stage for $I_f = 1.7A$, $V_f = 0.8V$	$V_f I_f$	1.36W
Switching losses in diode D_2 of flyback stage for $I_f = 1.7A$, $V_f = 0.8V$	$V_f I_f$	1.36W
Switching losses in diode of boost stage for $I_f = 0.2A$, $V_f = 0.8V$	$V_f I_f$	0.16W
Output power	$P_o = V_o \times I_o$	30W
Input power	$P_{in} = P_o + \text{losses}$	33.28W

From Table I, it is clear that the conduction losses occurred across the switching components is less than the switching losses. The efficiency can be calculated by the ratio of output power to input power and on substitution of the values, efficiency in discharging mode is 90.13%.

Table II: Losses in various components of converter II

Description	Related Equations	Value
Conduction losses in diode D_1 of flyback stage for $I_d = 1A$, $R_{don} = 0.001\Omega$	$I_d^2 R_{don}$	1mW
Conduction losses in secondary winding of flyback transformer for $I_s = 1A$, $R_s = 1\Omega$	$I_s^2 R_s$	1W
Conduction losses in diode of the boost converter stage for $I_d = 0.325A$, $R_{don} = 0.001\Omega$	$I_d^2 R_{don}$	0.105mW
Conduction losses in MOSFET of the output boost converter for $I_d = 0.45A$, $R_{don} = 0.11\Omega$	$I_d^2 R_{don}$	22.2mW
Switching losses in diode D_1 of flyback stage for $I_f = 1A$, $V_f = 0.8V$	$V_f I_f$	0.8 W
Switching losses in diode of boost converter stage for $I_f = 0.4A$, $V_f = 0.8V$	$V_f I_f$	0.32 W
Output power	$P_0 = V_0 \times I_0$	30W
Input power	$P_{in} = P_0 + \text{losses}$	32.15W

The efficiency can be calculated by the ratio of output power to input power and on substitution of the values, efficiency in discharging mode is 93.3%.

Table III: Conduction and switching losses

	conduction+ switching losses of converter configuration 1	conduction+ switching losses of converter configuration 2
$V_{AC} = 230 V_{RMS}, 50 \text{ Hz}$	3.28 Watts	2.15 Watts

Table IV: Converter Efficiency

	Efficiency of converter configuration 1	Efficiency of converter configuration 2
$V_{AC} = 230 V_{RMS}, 50 \text{ Hz}$	90.13%	93.3%

From Table-II, it is found that the total losses of converter configuration 2 is less than the losses of converter configuration 1 and therefore, the efficiency of converter 2 is higher than the efficiency of converter 1. Table IV gives the efficiency of the converters.

VIII. Comparison between converter [1] and converter configuration [2]

- In the flyback stage of converter configuration 1[1], there are two secondary windings and one primary winding in the transformer but in the flyback stage of converter 2 configuration, there are two primary windings and one secondary winding in the transformer.
- In the flyback stage of converter 1[1] configuration, there are three Mosfets, two diodes whereas, the flyback stage of converter 2 configuration consists of 2 Mosfets and only one diode which imply that in the converter configuration 2, the number of switching components is reduced.
- The conduction and switching losses are reduced in the converter 2, as the number of switching components is reduced.
- The efficiency of the converter 2 is more than the efficiency of converter 1[1] due to the reduction in conduction and switching losses.

Conclusion

Two different converter configurations with efficient electronic driver for lighting application have been presented in this work. The design for both the converter configurations has been carried out for a 30 W LED lamp. The conduction and switching losses of both the converters presented in this paper are reduced when compared with the conventional converter configuration as the diode bridge rectifier is eliminated. Therefore, the efficiency of the converters is increased. In the converter configuration 2, the number of switching components is minimized when compared with the converter configuration 1. Therefore, the efficiency of the converter configuration 2 is increased due to the reduction in conduction and switching losses. Further, a snubber circuit is implemented in both the converter topology to reduce the voltage stress across the switches due to leakage inductance at the primary side of the flyback transformer.

References

- [1] Garcia, D Gacio, M.A. Dalla-costa and A.J. calleja, "A Novel Flyback- Based Input PFC Stage for Electronic Ballasts in Lighting Applications", IEEE Trans. Ind. Electron., vol. 49, no. 2, March/April 2013.
- [2] Y. Jang and M. M. Jovanovic, "Bridgeless high-power-factor buck converter," IEEE Trans. Power Electron., vol. 26, no. 2, pp. 602–611, Feb. 2011.
- [3] W. Yan, S. Y. R. Hui, and H. Chung, "Energy saving of large-scale highintensity-discharge lamp lighting networks using a central reactive power control system," IEEE Trans. Ind. Electron., vol. 56, no. 8, pp. 3069–3078, Aug. 2009.
- [4] R. Orletti, M. A. Co, D. S. L. Simonetti, and J. L. de Freitas Vieira, "HID lamp electronic ballast with reduced component number," IEEE Trans. Ind. Electron., vol. 56, no. 3, pp. 718–725, Mar. 2009.
- [5] W. Kaiser, "Hybrid electronic ballast operating the HPS lamp at constant power," IEEE Trans. Ind. Electron., vol. 34, no. 2, pp. 319–324, Mar./Apr. 1998.
- [6] M. A. Dalla Costa, J. M. Alonso, J. C. Miranda, J. Garcia, and D. G. Lamar, "A single-stage high-power-factor electronic ballast based on integrated buck flyback converter to supply metal halide lamps," IEEE Trans. Ind. Electron., vol. 55, no. 3, pp. 1112–1122, Mar. 2008.

Author

Anjali.R.N was born in Davangere, Karnataka state, India in 1986, She received her B.E from Kuvempu university during 2008 in India. In July 2012, she joined MTech in power electronics department, Dayananda college of Engineering, Visvesvaraya Technological University, Karnataka state, India. Presently she is pursuing MTech IV semester, Dayananda College of engineering, Bangalore,

K.Shanmukha Sundar obtained his B.E and M.Tech from Mysore University and KREC (presently it is NITK), Mangalore University during 1990 and 1994 respectively in India. He has obtained Ph.D degree during 2010 under Visvesvaraya Technological University, Belgaum, Karnataka State, India.

Presently he is with the department of Electrical & Electronics Engineering of Dayananda Sagar College of Engineering, Bangalore, India. His areas of interest are in FACTS devices for Optimal Power Flow, Optimization of Power System, Power Electronic converters and Drives.