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Design of a Fully Differential Current Buffer (FDCB) based on a new Common Mode Feedforward (CMFF) based Common Mode Separation Technique

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Abstract

In this paper, a new approach, the advantages of which are simplicity, low voltage and power and high common mode currents rejection, is presented for implementing of FDCB. CMFF is one of the best choices to insert a fully differential current substractors (FDCS) into the FDCB's structure resulting in high CMRR without using negative feedback. The proposed circuit profits from current-mode and fully differential signal processing. Simulation results provided by the Hspice software in 180nm CMOS TSMC process clearly proves the advantages of this design. Furthermore, the layout is done by Cadence, the area of which is 53*25.2(um)2. In the post layout simulations, the CMRR and the positive and negative PSRR are 58.19 dB, 117.1 dB and 147.8 dB, respectively. Input and output resistance and their bandwidth are 49.26 Ω, 2.4 MHz, 634.9 kΩ and 2.19 MHz, respectively. The proposed circuit under supply voltages of ±0.7 V consumes low power of 152.5 uW. The results of the corner cases and Monte Carlo simulations indicate that the performance of proposed circuit is less sensitive to fabrication process and temperature.

Keywords: *current mode processing fully differential current (FDCB), common mode feedforward (CMFF), fully differential current subtractor (FDCS), low voltage, low power, wide bandwidth.*

1. Introduction

Th The design of current mode analog integrated circuit has recently gained popularity. Wide bandwidth, high slew rate, low voltage and low power operation and circuit simplicity are some of the advantages of the current mode circuits compared to voltage mode ones [1-3]. Low voltage operation of current mode circuits has gained more importance due to semiconductor technology down scaling issue [4]. This scaling has also led to popularity of mixed-mode design in system-on-chips which the digital and analog parts are developed on one chip. Therefore, analog designers have to also concern about power supply and ground fluctuations causing by switching operations of the digital part. As a result, low voltage, high CMRR and high PSRR current mode structures, are critically required. Current buffers are main building blocks of current mode signal processing circuits. Their main specifications are low input impedance, high output impedance and unity current gain. Some practical examples of which are as follows:

- They are used to isolate on-chip circuitry from large parasitic capacitances at the chip input pads to allow taking full advantage of the speed capabilities of the current-mode circuits [5].

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- The voltage mode circuits can be converted to their current mode counterparts using adjoint network theorem based on current buffers [6-7].
- Current buffers can be used in wide band data communication [8-9].
- Different types of filters and oscillators can be implemented using current buffers [10-11].
- Current buffers are used at input stage of the most current mode circuits [12].

As fully differential signal processing is commonly used in many fields mainly due to its innate immunity to common mode signals, clock feed through, interferences and other common mode disturbances [1], [13-14]. A fully differential current buffer is more useful specially in mixed signal design. The most popular types of current buffers are common Gate transistor and different types of current mirrors [15-17] which are employed in current mode circuits. second generation current conveyor (CCII) can also be used as current buffer; Due to using of voltage mode followers, mentioned current buffer lose the most benefits of the current mode processing. All above mentioned current buffers have the common problem which is single-input single-output resulting in the same response to both wanted and unwanted input signals.

In [19], common mode feedback is used to design fully differential current buffer based on common gate stages. In the structures including CMFB, stability condition should be maintained which complicates the design procedure [20-21].

In [22] three topologies were reported for fully differential current buffers that are shown in Fig. 1. In these topologies, multiple current buffers were used to subtract input signals. Some drawbacks of these topologies are: high chip area and power consumption, unbalanced input impedances (Fig. 1.a), lower output impedance (Fig. 1.b), needing matched blocks (especially in Fig. 1.c).

Appropriate combination of current mirrors along with common gate stage can also be used to design FDCB [23]. In this manner, it is very difficult to match the P type and N type current mirrors. Probable mismatches between the current mirrors result low CMRR and PSRR for the FDCBs employing this approach. Although the method used in [7], [24-25] for designing FDCBs was successful in reducing common mode currents, however the CMRR of which is very sensitive to transistor parameters.

Due to the increasing importance of the fully differential structures, in this paper a new common mode separation technique [12] is introduced to design simple and high CMRR FDCB. In the proposed FDCB a new structure of CMFF is used to insert a FDCS into the structure of the FDCB resulting in high CMRR without using negative feedback. Negative feedback is used to obtain low impedance inputs.

The organization of this paper is as follows: In section 2, proposed FDCB and the Circuit equations are presented. Simulation results for pre-layout and post-layout net lists are presented in section 3. Finally section 4 concludes this paper.

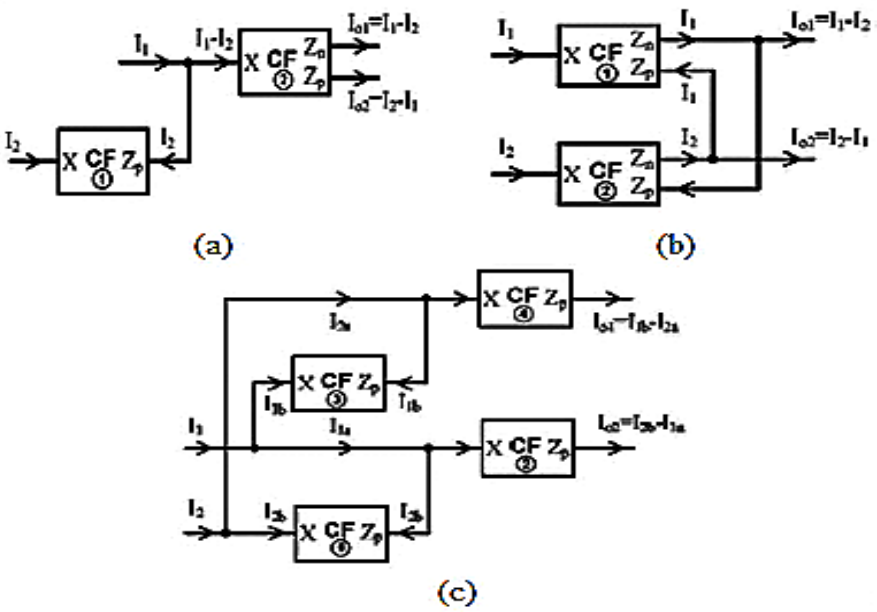

Figure 1: Fully differential current buffer topologies using single input-single output current buffers

2. proposed FDCB and the Circuit equations

Proposed circuit is shown in Fig. 2. Input impedance of the FDCB is decreased using negative feedback structure implementing by M1, M7 and M9 (M2, M8 and M10 on the other half of Crcuit). Loop gain of the negative feedback forces input nodes to have fixed voltage resulting in low input impedances. Performing small signal analysis, input impedance of each input terminal to ground can be written as the following:

$$R_{in\text{-}cm} = \frac{1}{g_{o1} + (g_{m1} + g_{o9}) \dfrac{g_{m7} + g_{o7}}{g_{o7} + g_{o9}}} \approx \frac{g_{o9} + g_{o7}}{g_{m1} g_{m7}} \tag{1}$$

In the Eq. (1), gmi and goi are transconductance and output conductance of i'th transistor. Due to the circuit symmetry, differential input impedance can be found as Eq. (2):

$$R_{in\text{-}d} = 2R_{in\text{-}cm} \approx \frac{2(g_{o9} + g_{o7})}{g_{m1} g_{m7}} \tag{2}$$

Therefore, determining proper values for gm and go of transistors, Eq. (2) results in a small enough differential input impedance. Due to constant gate voltage of M7 (and M8) all of the input current, including differential and common mode components, follows into the transistor M1 (M2).

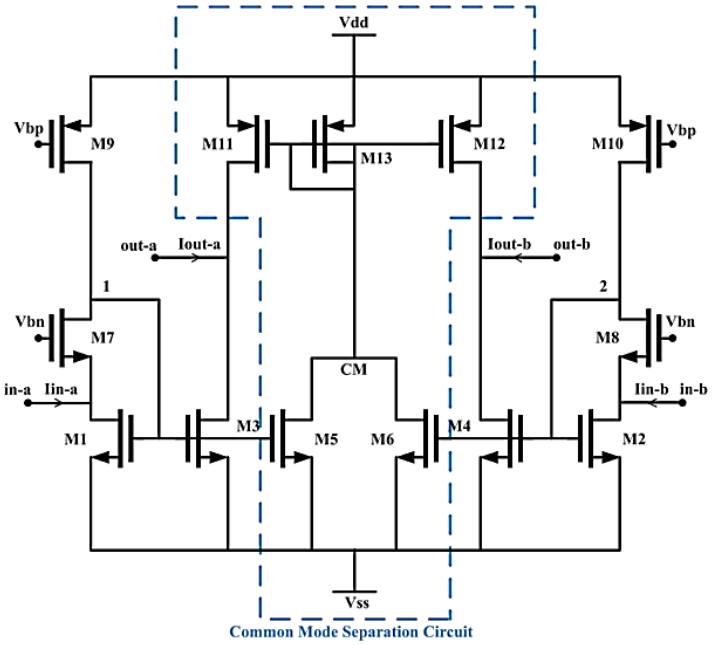

Figure 2: Proposed FDCB circuit

To transmit the differential and common mode currents passing through M1-M2 to the output terminals respectively with the gains of one and zero, a new structure is used. The structure is based on CMFF technique, implementing by the two groups of current mirrors: 1. The first group consists of current mirrors (M1, M3, M5) and (M2, M4, M6) at the two half of the circuit. 2. The second group consists of (M11-M13). Input current iina (iinb) passing through M1 (M2), is mirrored into the transistors M3 and M5 (M4 and M6) with the gain of α and α/2, respectively, by the action of the first group current mirror. Connecting drains of the transistor M5-M6, current signal equal to – α (iina+iinb)/2 is applied to the input of the second group current mirror. Finally mentioned current is mirrored into the transistor M11 (M12) with the gain of β, by the action of current mirror M11-M13 resulting in the removing common mode currents at the output nodes (outa and outb). It can be shown that the output terminal currents are for both of the common and differential mode as Eq. (3) and Eq. (4):

$$\mathrm{i}_{\mathrm{outb}} = \alpha\left(1-\frac{\beta}{2}\right) i_{inb} - \frac{\alpha.\beta}{2} i_{ina} + \alpha(1-\beta).I_b \tag{3}$$

$$\mathrm{i}_{\mathrm{outa}} = \alpha\left(1-\frac{\beta}{2}\right) i_{ina} - \frac{\alpha.\beta}{2} i_{inb} + \alpha(1-\beta).I_b \tag{4}$$

Where Ib is the biasing current of the circuit which is prepared by the transistors M9-M10. It can be seen from the equations above that the term of α(1-β)Ib is offset current of the output terminals. Now we can find the common mode and differential gains by using Eq. (3) and Eq. (4). Assuming differential input currents of iina = id and iinb = -id, output terminal's currents and differential mode current gain can be written as Eqs. (5) and (6):

$$i_{outb} = -\alpha i_d \Rightarrow A_{ib} = \alpha \tag{5}$$

$$i_{outa} = \alpha i_d \Rightarrow A_{ia} = \alpha \tag{6}$$

Assuming common mode input currents of iina = iinb = icm, output terminal's currents and common mode current gains can be written as Eqs. (7) and (8):

$$i_{outb} = \alpha(1-\beta)\, i_{cm} \Rightarrow A_{icmb} = \alpha(1-\beta) \tag{7}$$

$$i_{outa} = \alpha(1-\beta)\, i_{cm} \Rightarrow A_{icma} = \alpha(1-\beta) \tag{8}$$

determining α=β=1, differential and common mode gains and CMRR are respectively equal to one, zero and infinite, of which relations of input and output currents are like a FDCS, as are shown in Eqs. (9) and (10):

$$i_{outa} = \frac{i_{ina} - i_{inb}}{2} \tag{9}$$

$$i_{outb} = \frac{i_{inb} - i_{ina}}{2} \tag{10}$$

In the real case, the factors α and β aren't exactly equal to one. Therefore, CMRR's real equation can be obtained using Eqs. (5) to (8) as the following:

$$CMRR = \frac{A_{id}}{A_{icm}} = \frac{1}{1-\beta} \tag{11}$$

From the Eq. (11) it is clearly found that the β which is determined by the precision of second group current mirror, plays important role decreasing common mode gain.
The other important property of the FDCB is high output impedance. It can be shown that output impedance of the each output terminals of the circuit in Fig. 2, is as Eq. (12). It can be a proper value because of the small load resistor of the current mode circuit.

$$R_{out-cm} = \frac{1}{g_{o3} + g_{o11}} \tag{12}$$

3. Simulation Results

FDCB's performance has been verified by Hspice simulator using 180nm CMOS TSMC technology file. Simulations are performed while the same loads consisting RL=1kΩ and CL=0.1pF are placed at the output nodes. Besides, constant voltages of Vbn=245mV and Vbp=193mV are used to the biasing of the circuit. Table I shows transistor dimensions of the proposed FDCB. Fig. 3 to Fig. 7 show the curves resulting from the circuit simulations. Frequency response of the FDCB's differential current transmission is shown in Fig. 3, high bandwidth and low transmission error of which are clear.

Table 1: Transistors Aspect Ratios

Transistor	W/L (um)
M1-M4	18.36/1.53
M5-M6	9.18/1.53
M7-M8	20.43/1.08
M9-M10	6.03/1.62
M11-M13	55.71/1.89

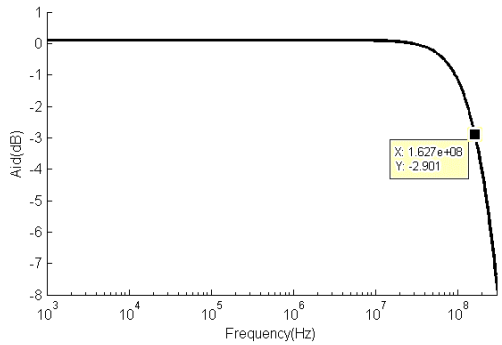

Figure 3: Frequency response of the FDCB's differential current transmission

Frequency response of the CMRR is shown in Fig. 4. It is clear that the CMRR has high value for a relatively wide band. Moreover, Fig. 5 shows positive and negative PSRRs of the circuit. It is clear that the proposed circuit is so insensitive to the power supply disturbance. Impedances of the each input and output terminal to ground versus the frequency is shown in the Fig. 6 and Fig. 7, respectively. From the Fig. 6, it can be seen that by the action of negative feedback, input impedance of the input terminals is decreased to 49Ω in low frequency. As it can be shown in Fig. 8, Layout of the proposed FDCB has been done by using Cadence in 0.18um TSMC 1P6M technology, the area of which is 53*25.2 (um)2. The layout has been designed as symmetric as possible to eliminate mismatches between the differential parts of the device.

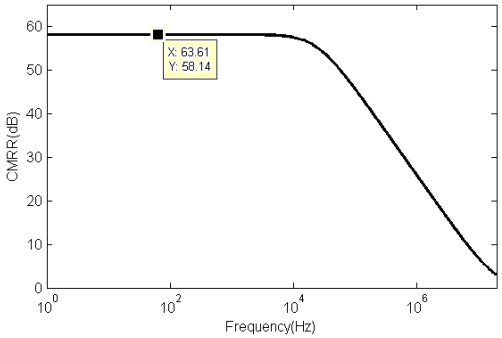

Figure 4: Frequency response of the CMRR for the proposed circuit.

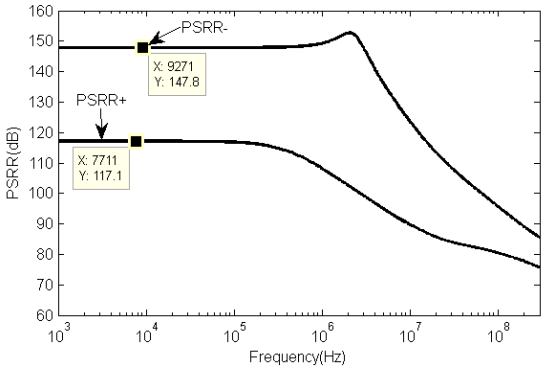

Figure 5: Frequency response of the positive and negative PSRRs of the FDCB.

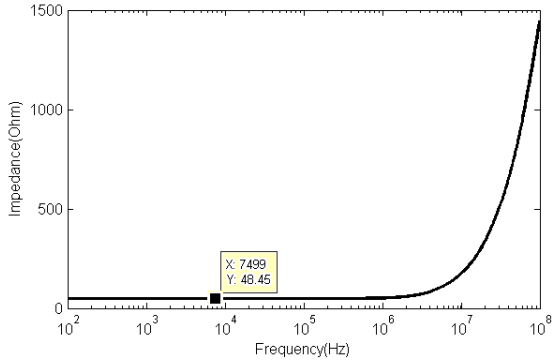

Figure 6: Input impedance of each input terminal to ground versus frequency.

To investigate the effect of mismatches on the CMRR performance of the proposed circuit, Monte Carlo simulations are performed by considering 1% mismatch in µ.Cox.W/L of transistors for 100 runs. The pre-layout and post-layout Monte Carlo simulation results are shown in Fig. 9.(a) and (b), respectively, the mean value of both of which are near 50.7dB. Monte Carlo simulation is also performed for the output and input resistance of the post-layout net list and the results are shown in Fig. 10.

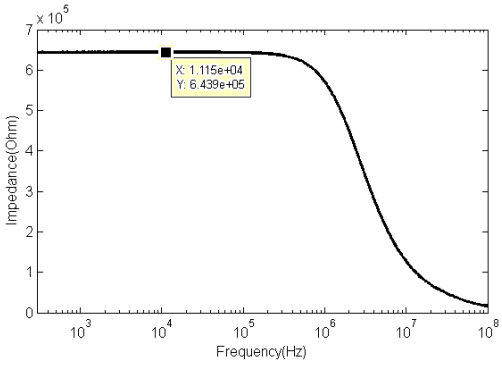

Figure 7: Output impedance of each output terminal to ground versus frequency.

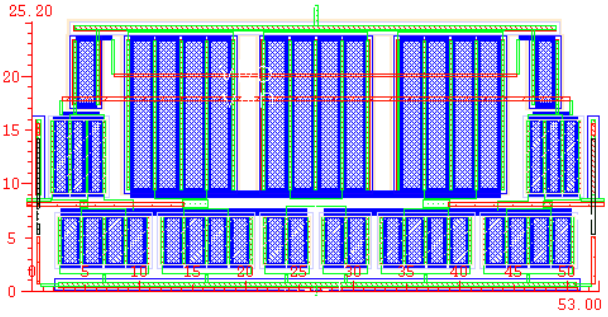

Figure 8: FDCB layout.

Table II summarize the performance of the CMIA resulting from pre-layout and post-layout HSPICE simulations. Moreover, corner case simulation results are studied and reported in Table III which shows a robust performance for the proposed FDCB.

A comparison between the proposed FDCB and some other reported works is given in Table IV. The high CMRR and low input impedance in [24] are very sensitive to process variation. Comparing the other work, proposed FDCB Simultaneously profits from low power, low voltage, wide bandwidth and high CMRR properties. In addition to all of these, proposed FDCB has a simple and symmetric structure with low number of transistor.

Conclusion

This paper proposes a new structure of common mode feedforward (CMFF) technique to design a simple, low voltage, low power and high CMRR fully differential current buffer (FDCB). Actually, high CMRR is obtained by inserting a fully differential current subtractor into the structure of FDCB. As the simulation results show, proposed CMFF based common mode separation technique can be used in current mode signal processing as a simple and effective method.

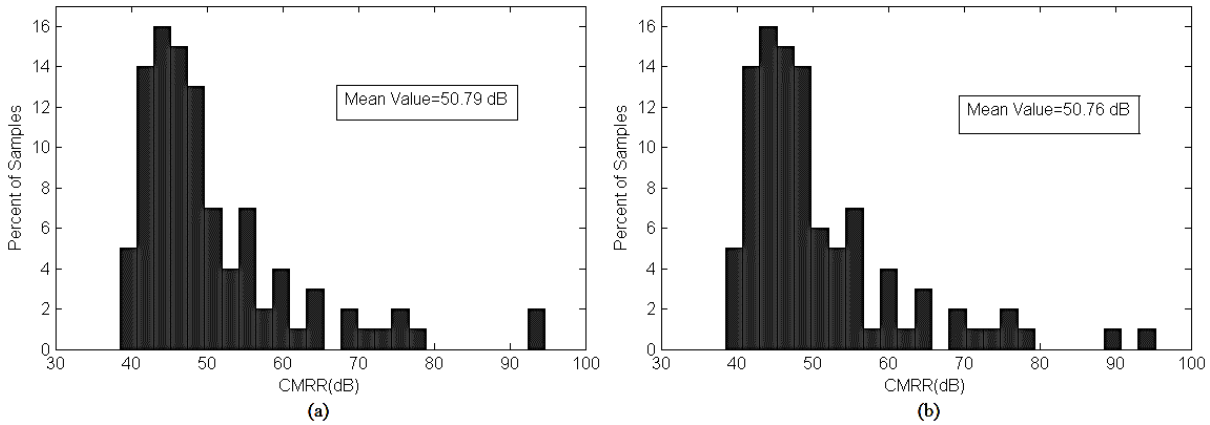

Figure 9: Monte Carlo simulation result of CMRR for (a) pre-layout and (b) post-layout simulations

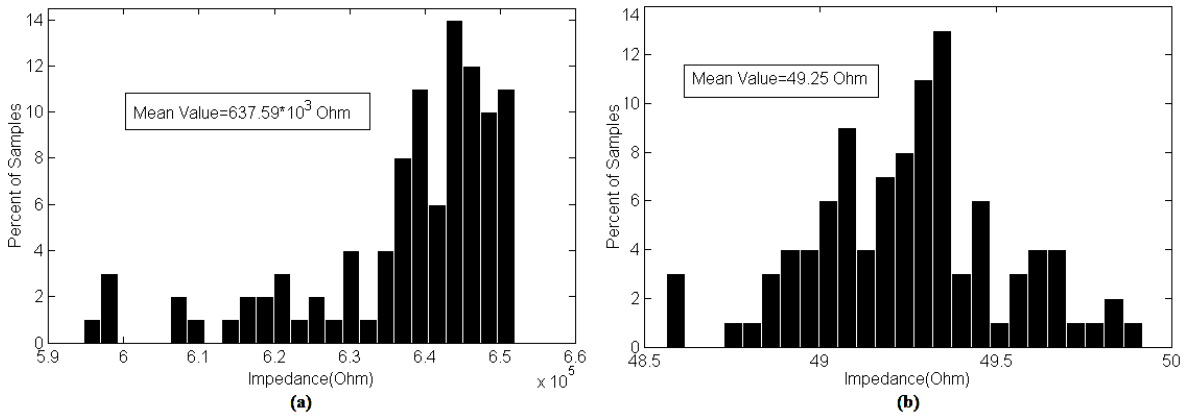

Figure 10: Monte Carlo simulation results of (a) output impedance and (b) input impedance.

Table 2: Proposed FDCB Specifications

Specification	Pre-Layout Simulation Results	Post-Layout Simulation Results
Ad(dB)	0.1069	0.1066
F-3dB(MHz)	162.7	159.1
CMRR(dB)	58.14	58.19
fT of CMRR (at which CMRR=0dB)	215 MHz	158.8 MHz
Input impedance	48.45 Ω	49.26 Ω
Output impedance	643.9 kΩ	643.9 kΩ
PSRR-(dB)	147.8	147.8
PSRR+(dB)	117.1	117.1
Supply Voltage	±0.7 V	±0.7 V
PD(uW)	152.5	152.5

Table 3: Corner Case Simulation Results of the Proposed FDCB

Corner	Sim-type	Ad(dB)	F-3dB(MHz)	CMRR(dB)	fT of CMRR (at which CMRR=0dB)	Input impedance	output impedance
SS	pre-Layout	0.1233	144	42.23	180.8 MHz	33.11 Ω	758 kΩ
FS		0.1125	153	49.22	190.6 MHz	176.46 Ω	618.5 kΩ
SF		0.121	170.3	45.56	235.6 MHz	25.86 Ω	526.2 kΩ
FF		0.1032	180.7	46.22	242 MHz	110.93 Ω	426.9 kΩ
SS	Post-Layout	0.1231	140.9	42.24	145.8 MHz	33.9 Ω	758.1 kΩ
FS		0.1123	149.4	49.19	152 MHz	177.67 Ω	618.6 kΩ
SF		0.1207	166.7	45.58	175.2 MHz	26.64 Ω	526.2 kΩ
FF		0.1029	176.9	46.2	175 MHz	111.89 Ω	426.9 kΩ

Table 4: Comparision Between the Proposed FDCB and Some Other Works

Refs	Tech Node (CMOS)	Ad		CMRR	Supply Voltage	PD(mW)	Rin(Ω) Ro(Ω)	Results
		Value (dB)	F-3dB(MHz)					
[23]	2um	6	1.25	62dB	5V	3	2.5k 10M	Measured
[19]	0.8um	-6.02	>37	38dB	5V	22	213 68k	Sim (schematic)
[22]	0.18um	NA	57	50dB	±1.5V	NA	- -	Sim (post-layout)
[24]	0.18um	0.1	369	98dB	±0.75V	0.135	8.48 -	Sim (schematic)
[12]	0.18um	0.172	144	32.9dB	1.4	0.179	- -	Sim (schematic)
Prop	0.18um	0.1069	162.7	58.1dB	±0.7V	0.152	49.2 643.9k	Sim (post-layout+ monte carlo)

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