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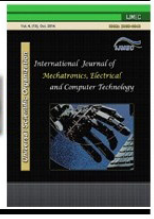

A 0.88nS Settling Time 115µV Settling Error with 68.18dB SNDR Continuous-time Common-Mode Feedback (CMFB) Circuit in 180nm CMOS Technology

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Abstract

This paper proposes a new high-speed and high-linear continuous-time Common-Mode Feedback Block (CMFB) circuit. The main purposes of the proposed idea are to increase the speed and linearity of the CMFB, reliably. Utilizing the worst case simulation on the proposed CMFB circuit, the output voltage can be settled in the preferred level just after 0.88nS. As simulation results prove that, at 1.8 V supply voltage and 100 MS/s sampling rate with a Nyquist input (49.9MHz), the amplifier achieves a SNDR of 68.18dB and a consistent ENOB of 11.07bit consistently. The power consumption of the suggested CMFB is 374µW with the power supply of 1.8 volts, also the settling time error is 115µV. Moreover, as simulation result demonstrates, exerting the reference voltage (Vref) from 0.6 to 1.35 volts the suggested circuit be able to adjust the output value in the suitable level with low error properly. Also, DC gain of the amplifier is 67dB, and the phase margin is 60 and 72.5 degree without and with considering the capacitor load at the output of the amplifier respectively, meanwhile, for this case the unity gain bandwidth is 1.5GHz and 886MHz correspondingly. It is notable that, 1pF capacitor load is applied to the output nodes of the amplifier. The chip area of the proposed CMFB is 16.2µm*22µm, also for operation correctness of the CMFB, Monte-Carlo simulations are applied to the amplifier too, evidently. Simulation results are done using the HSPICE BSIM3 model of a 0.18µm CMOS technology.

***Keywords:** Amplifier, Common-mode feedback, Power consumption, Telescopic, High-speed*

1. INTRODUCTION

A Common-Mode Feedback Block (CMFB) circuit is a network to sense the common-mode voltage, relate it with an appropriate reference, and to feedback the correct common-mode signal with the purpose to cancel the output common-mode current component and to fix the DC outputs to the desired level [1, 2, 5, and 6]. Figure 1 illustrates the basic conceptual structure of the CMFB [6]. In addition to, the CMFB circuit is a fundamental circuitry for a fully differential system. Without CMFB, the transistors in the system may easily drift away from saturation region due to mismatch and other process tolerances and cause a system malfunction, especially in low supply voltage applications where the voltage headroom to keep transistors in the saturation region is very small[7,

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10, 11, 19]. Perfectly, the CMFB circuit should only response to CM voltage changes but not differential voltage changes; otherwise, the output dynamic range and linearity of the FDAs would be degraded [10, 20]. Modern advances in current-mode signal processing have confirmed that continuous-time current-mode circuits are good alternatives for high-speed signal processing. However, continuous-time differential current-mode circuits introduce unique requirements for common-mode feedback circuits [6]. Then differential nodes in current-mode circuits normally have high impedances, the impedance of the CMFB may have a significant effect on the node impedance. Variation in the node impedances in current- mode circuits usually results in changes in the locations of the poles and zeros of the system's transfer function, which impacts the system performance [4, 8].

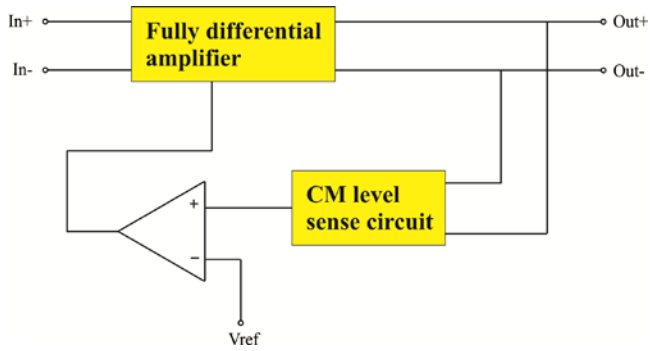

Figure 1: The basic conceptual structure of the CMFB

Stability problems may also occur too. If the CMFB itself has another low-frequency pole, this CMFB circuit may be unstable. Accordingly, common-mode feedback current-mode circuits must satisfy the requirements of very high input and output impedances and stable response [2, 9, and 15]. Also, there are three different types of CMFB circuits. Resistor averaging circuit(R-C), switched-capacitor averaging circuit, and differential difference amplifier (DDA) [3, 6, 9, 10, 13, 16, 17, 18].

In this paper, a new high speed and high linear continuous-time Common-Mode Feedback Block (CMFB) circuit is presented. Which is able to adjust the output voltage of fully differential amplifiers with very small output common-mode error and properly large linear input range as well. Furthermore, the aims of the proposed idea are to increase the speed, decrease the settling time error and improve the linearity of the common-mode feedback circuit. The proposed paper is organized as follow: Proposed common-mode feedback is presented in section 2. In section 3 simulation results of the paper are specified and finally, section 4 concludes the paper.

2. THE PROPOSED COMMON MODE FEEDBACK BLOCK

Figure 2 indicates the structure of the proposed common-mode feedback. It is noteworthy that, the speed of each CMFB is reversely relative to the sum of parasitic capacitors which are in the output of the CMFB circuit and make delay for the feedback signal. In the proposed method, the basic idea is to eradicate the diode-connected transistors in the conventional DDA CMFB which applies the error correction signal to the folded cascode or telescopic op-amps. Since the diode-connected transistor generates an enormous delay in the feedback signal's path. As a result, by removing this transistor, the speed of the CMFB circuit will be increased extremely [1, 6]. It is notable that, the proposed idea is applicable to apply on every fully differential amplifier, however, in this paper it is utilized on a telescopic amplifier. Figure 3 shows the simple telescopic amplifier. It is obvious that the telescopic architecture is a good candidate for a low power, low noise and high gain OTA, of course, the performance of simple telescopic OTA is limited by its input and output voltage

swing [1, 6, and 14]. Therefore, a new high linear and fast CMFB circuit is presented in this paper which is able to adjust the output voltage of fully differential amplifiers with very small output common-mode error and properly large linear input range as well.

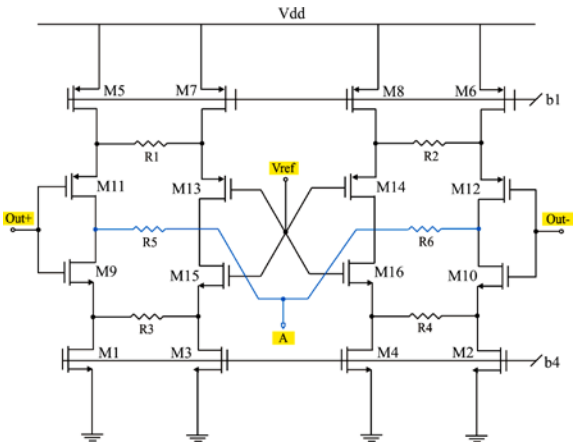

Figure 2: The proposed CMFB circuit

The transistors of M1- M8 are the current source biases and b1-b2 are the bias voltages of the circuit, also, the M9-M12 can play the function of the sensors of the proposed CMFB which the output voltages of the differential amplifiers are applied to the gate terminals of the mentioned transistors as well. Meanwhile, the resistors R5 and R6 are the actuators of the CMFB. In order to compare the output value of the differential amplifiers with the preferred value, the reference voltage (Vref=Vdd/2) is applied on M13-M16 suitably. The operation of the proposed CMFB is as follows: if the output common- mode voltage of the differential amplifier is supposed to high (maximum voltage), in this case, the actuators M9 and M10 will be active (work in saturation region) and M11 and M12 deactivate (work in the cut-off region) respectively. So, through the sensors (R5 and R6) the output result of the CMFB is feed backed to the amplifier which is shown in the node of A simply. Also, if the output common mode voltage of the differential amplifier is assumed to low (minimum voltage), in this condition, the actuators M11 and M12 will be active (work in saturation region) and M9 and M10 deactivate (work in cut-off region) respectively. The important point is here, if the output common mode voltage of the differential amplifier is chosen near to reference voltage (Vref) in that time, all of the transistors work in the saturation region and adjust the output voltage to the desired value as well. Meanwhile, for improving the linearity of the proposed CMFB circuit the resistors R1-R4 are exerted in the source terminals of the M9-M16 simply, and the typical values of the mentioned resistors are considered around 50Ω.

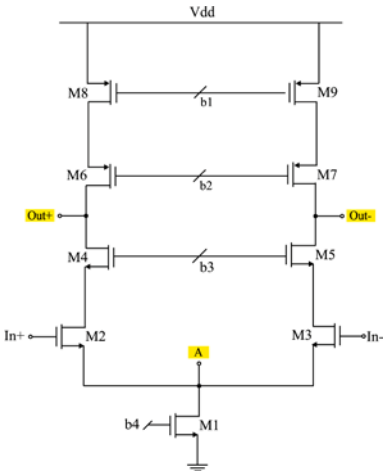

Figure 3: A simple telescopic amplifier

Similarly, the output swing voltages of the proposed CMFB are presented in (1), where $\Delta V_{1,9}$ and I are overdrive voltage and output current of the mentioned transistors in the suggested CMFB, correspondingly. The proposed idea is an appropriate option for low voltage applications too because it needs just fewer voltage to start its performance. Furthermore, the another key feature of the mentioned CMFB circuit is widely dynamic range voltage with low error, it means that if Vref adjusted near to 0.6 to 1.35 volt, the output voltage of the main circuit can be settled at the desired level, owing to that, the voltage of the output nodes remains near to preferred amount as well. Also, all of the transistors operates in the saturation region.

$$Output\ Swing = Vdd - (R_5 * I) - 2\Delta_{v1,9} \quad (1)$$

3. SIMULATION RESULTS

The simulation results of the proposed circuit are presented in this section. As simulation results prove, applying the reference voltage (Vref) from 0.60 to 1.35 volts, the proposed common-mode voltage is the ability to keep the output voltage in desired value suitably. Figure 5 and 6 indicate the bode plots of the CMFB loop of the amplifier without and with load capacitor respectively. Which the unity gain bandwidth is 1.5GHz and 886MHz for the CMFB loop, and the phase margin is 60° and 72.5° consistently, also the DC gain is 67dB as well. Also, for this case, the 100 irritation Monte-Carlo simulation is applied by 5%varation of transistors threshold voltage which is depicted in figure 7. Transient response of the output common-mode voltage is shown in figure 8, as it is clear in figure 8, applying the worst case simulation on the proposed CMFB circuit, the output voltage can be settled in the desired level just after 0.88nS. Moreover, Monte Carlo simulation results are applied to the transient response of the output common-mode voltage for 4% variation of transistors threshold voltage and temperature variation on the proposed CMFB which are shown in figure 9 and 10 respectively. Simulation results verify that even with these possible variations the proposed circuit offers estimated performance. The output telescopic amplifier FFT spectrum is depicted in figure 11. To apply a 49.9MHz input sinusoidal frequency at 100MHz sampling frequency with the amplitude of 1mV results in an output THD less than -68dB. It is noteworthy that, utilizing the proposed CMFB the linearity of the amplifier is improved well. Finally, the layout of the suggested CMFB circuit is shown in figure 12. The circuit has been designed in a typical 0.18 µm CMOS process with a power supply of 1.8V and simulated by HSPICE software using level 49 parameters (BSIM3v3).

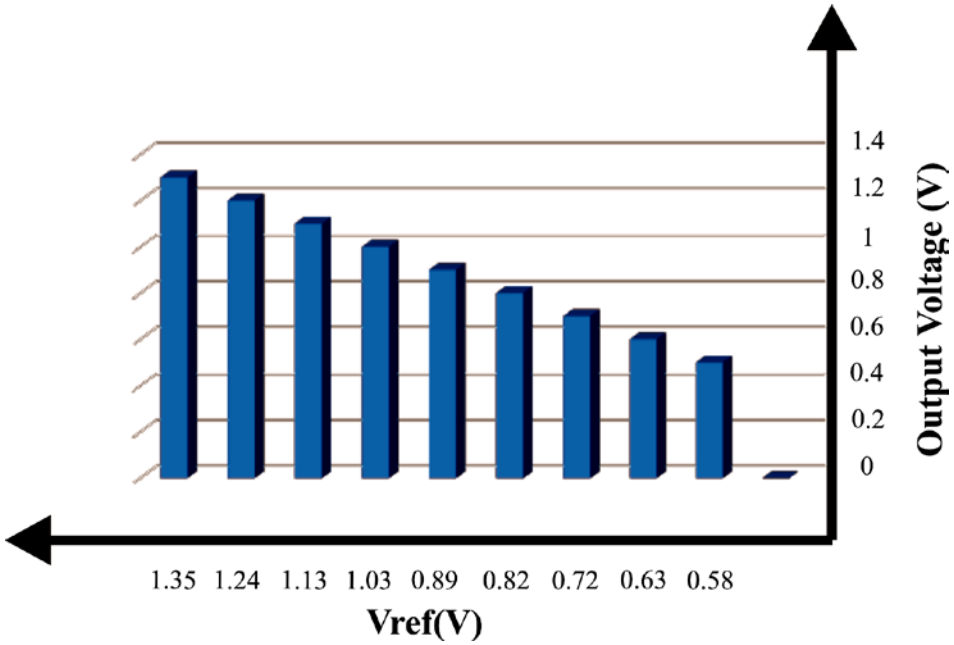

Figure 4: Output common-mode voltage error: 0.60<Vref<1.35.

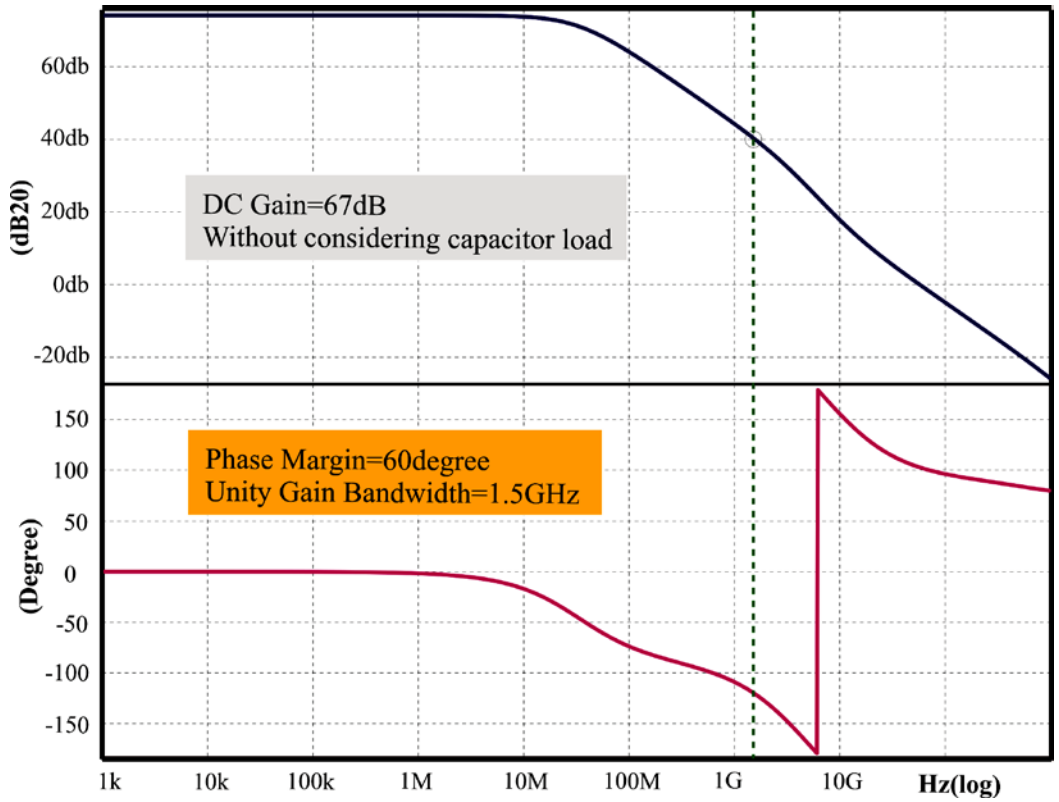

Figure 5: Loop gain frequency response of the proposed CMFB circuit without considering capacitor load

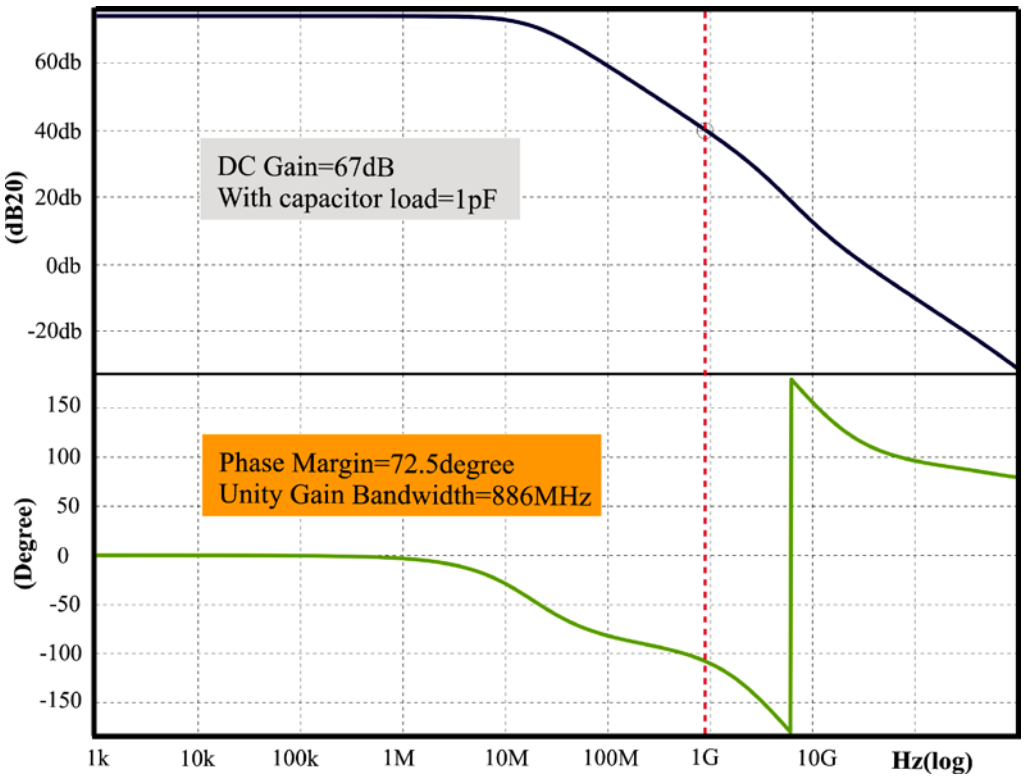

Figure 6: Loop gain frequency response of the proposed CMFB circuit with considering capacitor load

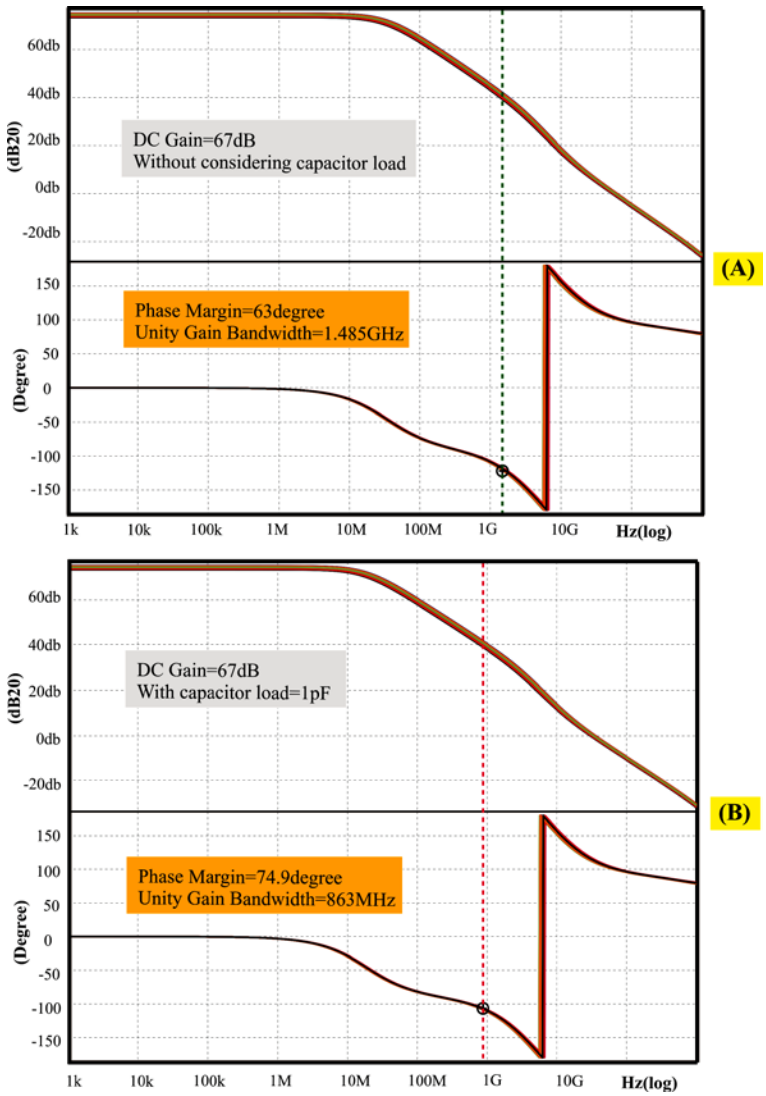

Figure 7: Loop gain frequency response of the proposed CMFB by applying Monte-Carlo simulation 5%varation of transistors threshold voltage

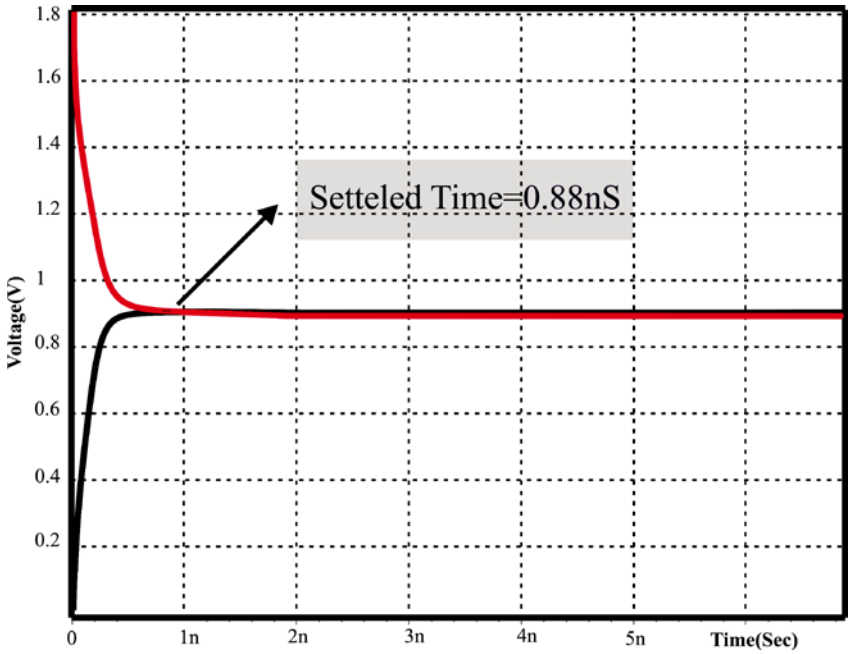

Figure 8: Transient response of the output common-mode voltage

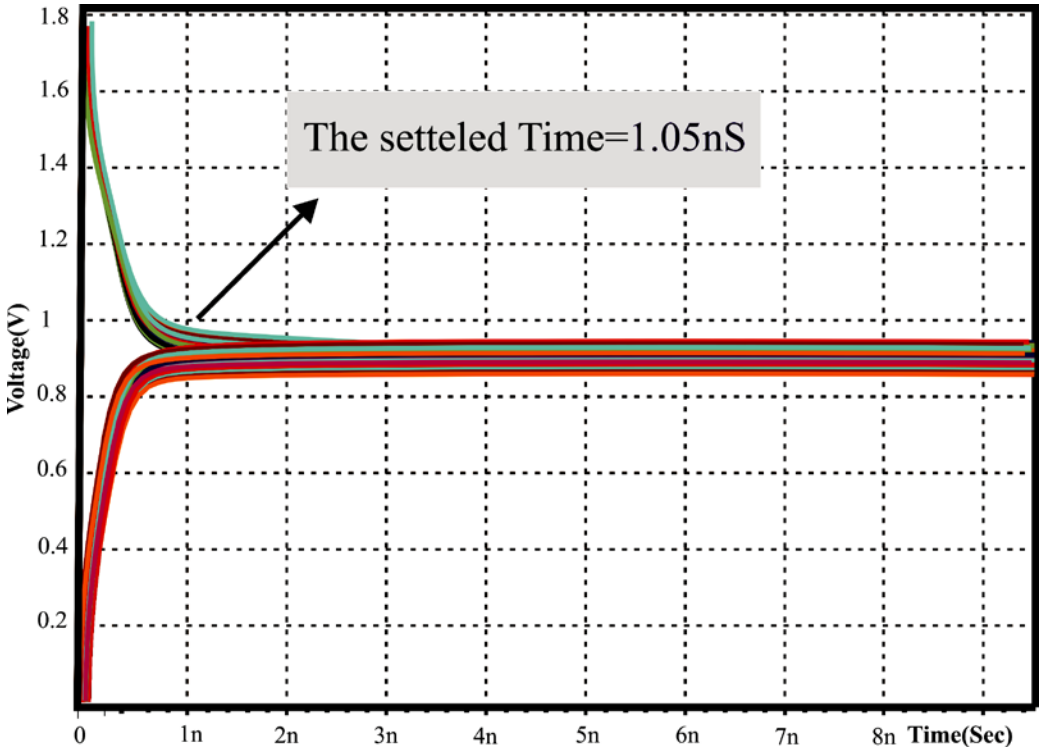

Figure 9: Transient response of the output common-mode voltage by applying the Monte-Carlo simulation 4%varation of transistors threshold voltage

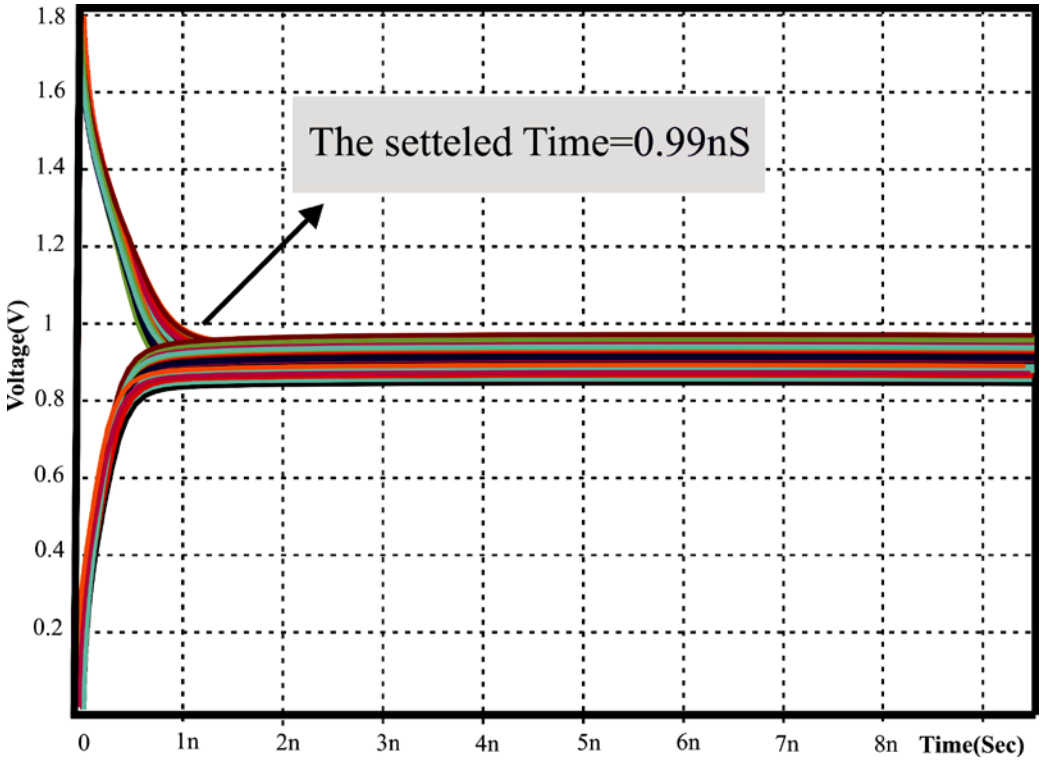

Figure 10: Transient response of the output common-mode voltage by applying the Monte-Carlo simulation temperature variation from -50°C to +100°C

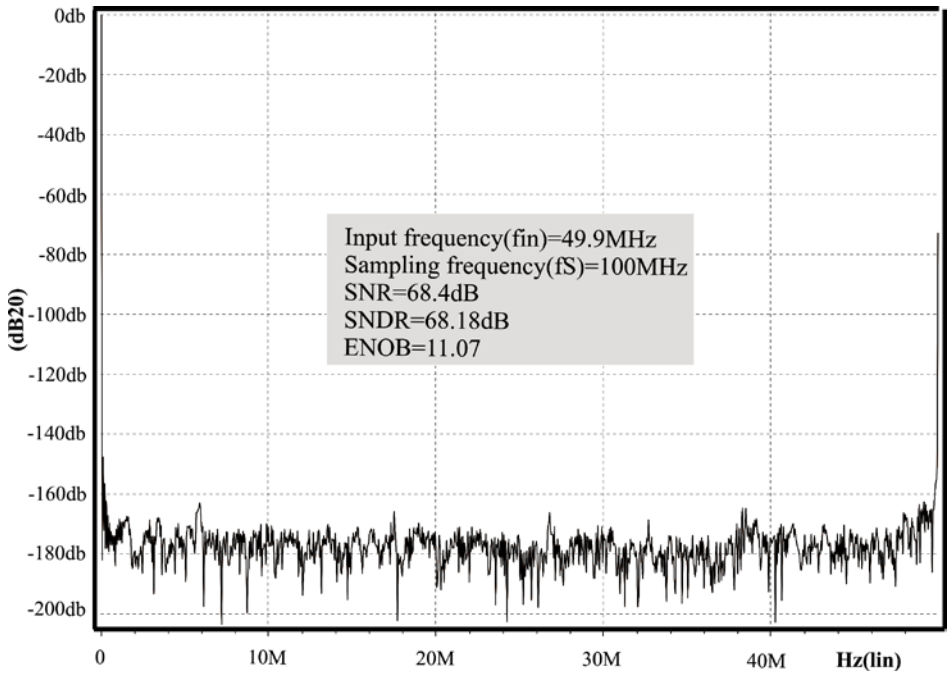

Figure 11: output FFT spectrum of the amplifier

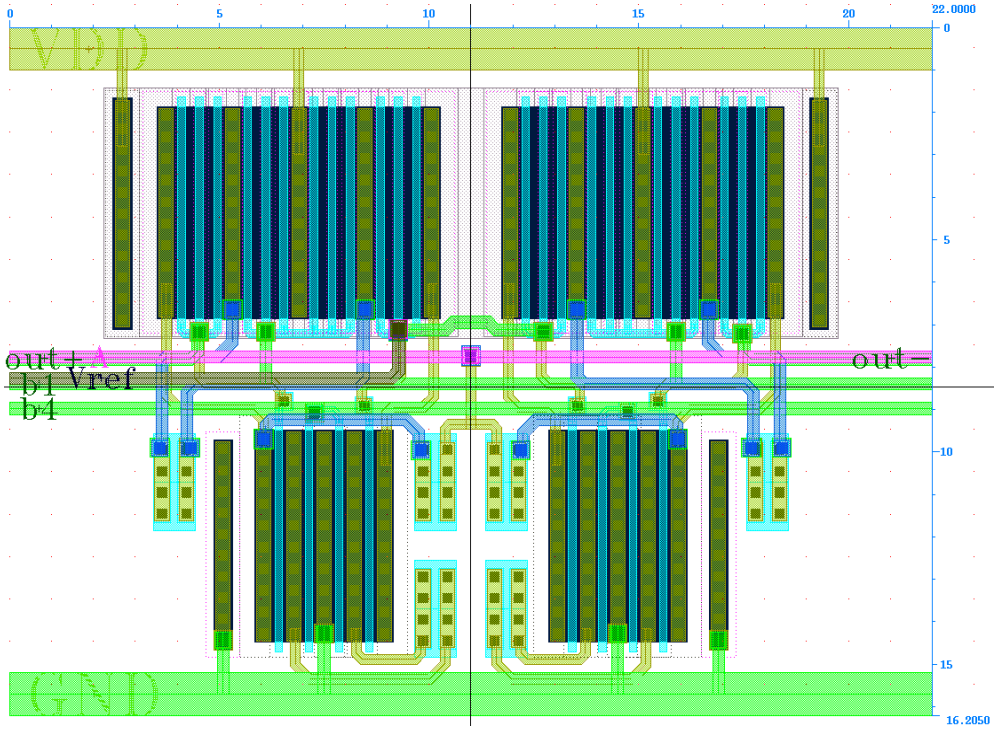

Figure 12: Layout of the proposed CMFB

CONCLUSION

A new simple and reliable technique to design a continuous-time common-mode feedback circuit is presented in this paper. The main purposes of the proposed idea are increasing the speed, decreasing the output settling time error and improving the linearity of the common-mode feedback circuit. The settling time and the settling error of the proposed CMFB are just 0.88nS and 115µV respectively. Besides, the proposed CMFB circuit has an extensive dynamic range voltage to set the output in the desired value too. As simulation result indicates the proposed circuit can adjust the output in the reliable value by applying the Vref from 0.6 to 1.35 volts suitably. The power

consumption of the proposed circuit is 374µW with the power supply of 1.8 volts also Table 1 compares this work with the similar previous one. Simulation results are performed using the HSPICE BSIM3 model of a 0.18µm CMOS technology.

Table 1: Comparison Table

	[6]	[10]	[13]	This work
Technology	0.35µm	0.13µm	0.18µm	0.18µm
Supply Voltage	3.3V	1.8V	0.9V	1.8V
Power consumption	-	1.8mW	-	374µW
Settling error	0.35mV	-	0.9mV	115µV
Settling speed	1.1nS	-	30nS	0.88nS
Unity gain bandwidth	-	450MHz	39.7MHz	886MHz
Phase margin	-	70°	68°	72.5°
DC gain	-	85dB	62.3dB	67dB
Capacitor load (CL)	-	1pF	4pF	1pF
THD	-	-40dBc	-	-68dBc
Chip area	-	-	-	16.2µm*22µm

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