Vol. 10(36), Apr. 2020, PP. 4543-4556

Contents list available at IJMEC

International Journal of Mechatronics, Electrical and Computer Technology (IJMEC)

Journal Homepage: www.aeuso.org

PISSN: 2411-6173 - EISSN: 2305-0543

Study on the Sigma Delta ADC Modulators Based on Signal to Noise Ratio (SNR) and Effective Number of Bits (ENOB) Parameters

Sina Mahdavi*[1], Arvin Mohammady[1], Faeze Noruzpur[2], Shima Tayyeb Ghasemi[2] and Mohammad Madadpour Inallou

[1]*Department of Electrical Engineering, Technical and Vocational University of Tabriz, Tabriz, Iran*

[2]*Department of Microelectronics Engineering, Urmia Graduate Institute, Urmia, Iran*

***Corresponding E-mail:** mahdavi9099@yahoo.com*

Abstract

In this paper, the Signal to Noise Ratio (SNR) and Effective Number of Bits (ENOB) parameters of the different types of the Sigma Delta ADC Modulators are studied and discussed, comprehensively. The CIFF structure of first, second and third orders with considering the different OSR are presented. Meanwhile, the MASH 1-1, MASH 2-1, and MASH 1-1-1 structures are analyzed and simulated, carefully, too. It is noteworthy that, as simulation results prove, the SNR and ENOB of each modulator is dependent on the value of the Order, OSR, and Quantizer bit parameters, extremely. For this case, in the design of the sigma-delta modulator, the designers must be considered and selected the suitable value for the mentioned parameters, carefully. Also, among of the presented modulators in this paper, the first order CIFB structure has minimum SNR and MASH 1-1-1 structure with good optimization has the maximum SNR, respectively. Finally, simulation results of the different orders and kinds of the DSM are compared in the comparison tables, too. Simulation results of the proposed paper are simulated using the MATLAB software.

Keywords: *ADC, Delta Sigma, DSM, MASH, Modulator, CIFF*

I. Introduction

Different types of ADCs are available nowadays, usually successive approximation or dual slope ADC is used when high resolution is chosen [1, 5, 10, 11, 13, 15, 19, 21, 25, 26, 27, 28]. However, use of this family of ADCs is ineffective in many applications as it requires trimming to achieve higher accuracy [6, 9, 15, 20]. Its widespread use is also limited due to the complexity in the design of high precision sample and hold circuits [1, 2, 3, 4, 8, 13,15, 17, 18, 21, 25, 27, 28, 30, 32]. Sigma-delta is an implementation method to realize converter with high accuracy [13, 15, 16, 26, 28, 29]. It uses the over sampling principle to compress the energy of quantization noise largely in the signal frequency band, and finally, through the down-sampling accomplished by digital decimation filter, so the higher SNR can be got [2, 4, 27, 30]. Comparing with the converters with other structures, sigma-delta ADC has the advantages of high accuracy, high linearity, large dynamic range and so on [5, 6, 7, 10, 12, 15, 19, 20]. The oversampling ADCs sample analog signal with higher sampling rate than Nyquist rate, which is usually expressed through OSR [1, 3, 4,

Article History:
Received Date: Apr. 11, 2019
Accepted Date: Aug. 01, 2019
Available Online: Apr. 01, 2020

23, 24, 28, 30]. Also, the oversampling converters use digital signal processing techniques instead of the complex and precise analog signal processing techniques exploited in the Nyquist rate converters [2, 7, 10, 11, 13, 14, 25, 27]. Generally, a Sigma-Delta ADC consists of a digital section and an analog section. The digital filter along with the decimation filter forms the digital section. Analog section of sigma-delta modulator consists of an analog differencing unit, integrator, comparator and one-bit DAC [5, 11, 13, 16, 24, 25]. The main characteristics of Sigma Delta ADC [1, 3, 4, 6, 9, 11, 12, 14, 15] can be summed up as Oversampling, Noise Shaping, and Decimation. Oversampling means the technique of sampling the input signal at a frequency much greater than the Nyquist frequency [1, 2, 4, 5, 13, 14, 17, 18]. This method of sampling signals greatly reduces the quantization noise in the band of interest [9, 11, 16, 25]. Meanwhile, in the sigma-delta converter, the noise shaping filter distributes the quantization noise in such a way, which is very low, in the required band of interest. Decimation [1, 2, 3, 8] is the act of reducing the data rate down from the oversampling rate without loss of information. A digital filter is also used to remove signals and noise that are outside the band of interest [5, 6, 12, 17, 18, 19, 22, 31]. In this paper, the Signal to Noise Ratio (SNR) and Effective Number of Bits (ENOB) parameters of the different types of the Sigma Delta ADC Modulators, are studied and discussed, comprehensively. It is notable that, among of the presented modulators in this paper, the first order CIFB structure has minimum SNR and MASH 1-1-1 structure with good optimization has the maximum SNR, as well.

The proposed paper is organized as follows. Basic building block of Sigma Delta ADC is presented in section II. Section III describes the system level model simulation of CIFF first, a second and third order of the Sigma Delta ADC by using MATLAB. System level model simulations of MASH 1-1 (Two Stage), MASH 1-1-1 (Three Stage) and MASH 2-1 (Two Stage) of the Sigma Delta ADC are advocated in section IV. Simulation results of the paper is presented in section V and finally, section VI concludes the paper.

II. Basic Building Block of Sigma Delta ADC

Principally, a sigma-delta ADC consists of an analog section and a digital section [1, 5, 6, 7, 11, 19, 20, 22, 25, 31, 32] which is indicated in Fig. 1. Meanwhile, analog section of sigma-delta modulator consists of an analog differencing unit, comparator, integrator and one-bit DAC. The digital filter together with the decimation filter forms the digital section [1, 2, 3, 4, 5, 8, 13, 14, 15, 16, 21, 24]. Usually, sigma-delta ADCs are used in audio systems, industrial weight scales, Data Acquisition systems and precision measurement devices [1, 3, 6, 8, 10, 11, 12, 13, 19, 27].

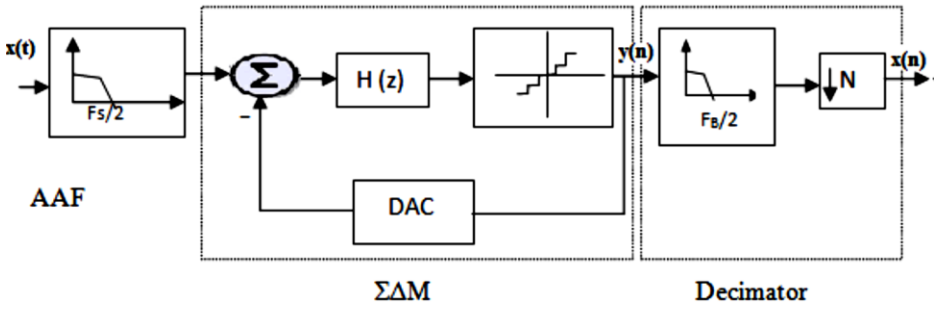

Fig. 1. Sigma Delta ADC Block Diagram [8]

III. System Level Model Simulation of CIFF First Second and Third order of the Sigma Delta ADC using in MATLAB

The system level CIFB architecture of the First-order Sigma Delta ADC is shown in Fig. 2. The FFT spectrum of Single-bit and Multi-bit quantization first order sigma-delta system level with considering OSR=256 are depicted in Fig. 3 and Fig. 4, respectively.

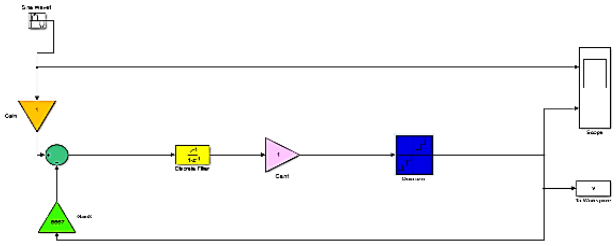

Fig. 2. The system level CIFB architecture of the First-order Sigma Delta ADC

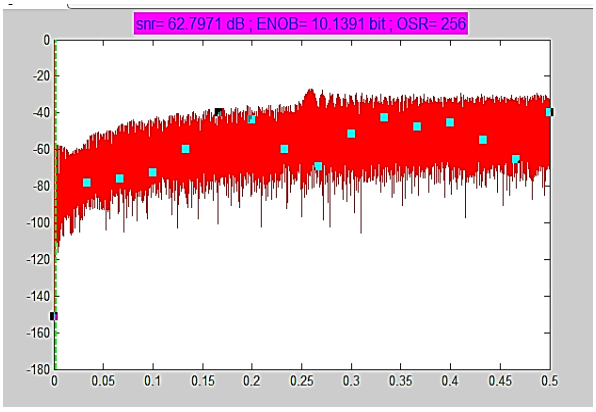

Fig. 3. The FFT spectrum of Single-bit quantization first order sigma-delta with considering OSR=256

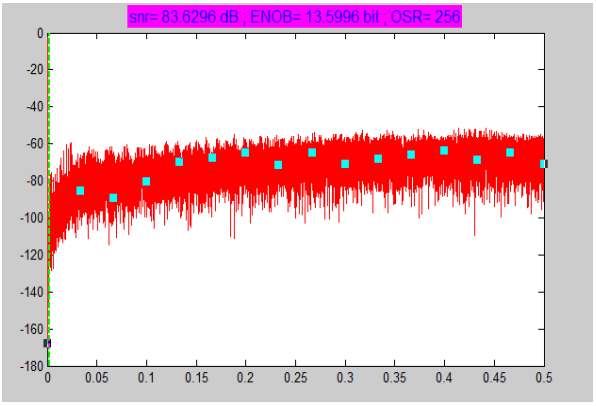

Fig. 4. The FFT spectrum of Multi-bit quantization first order sigma-delta with considering OSR=256

Also, the system level CIFF architecture of the Second-order Sigma Delta ADC is presented in Fig. 5. The FFT spectrum of Single-bit and Multi-bit quantization second order sigma-delta system level with considering OSR=256 are depicted in Fig. 6 and Fig. 7 respectively.

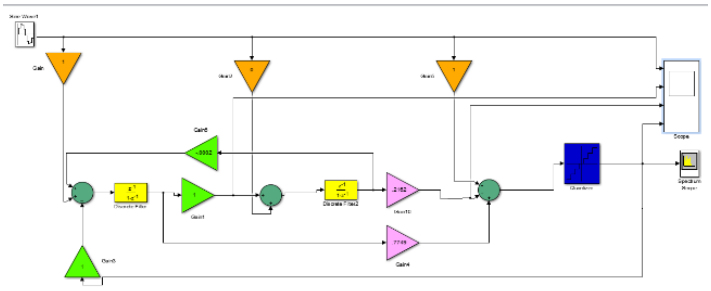

Fig. 5. The system level CIFF architecture of the Second-order Sigma Delta ADC

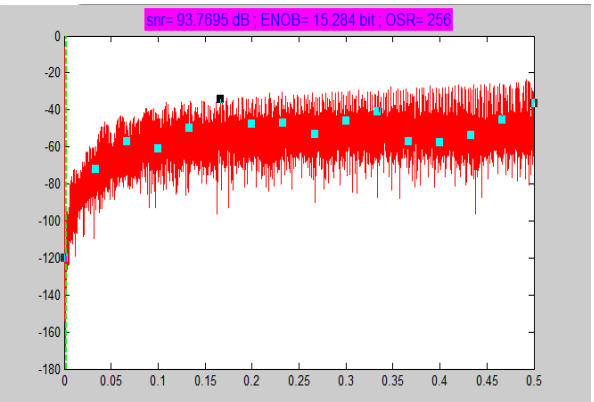

Fig. 6. The FFT spectrum of Single-bit quantization second order sigma-delta with considering OSR=256

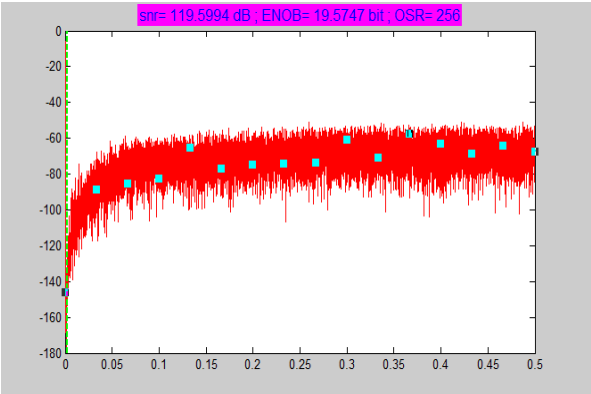

Fig. 7. The FFT spectrum of Multi-bit quantization second order sigma-delta with considering OSR=256

Meanwhile, the system level CIFF architecture of the Third-order Sigma Delta ADC is depicted in Fig. 8. The FFT spectrum of Single-bit and Multi-bit quantization third order sigma-delta system level with considering OSR=256 are depicted in Fig. 9 and Fig. 10, respectively.

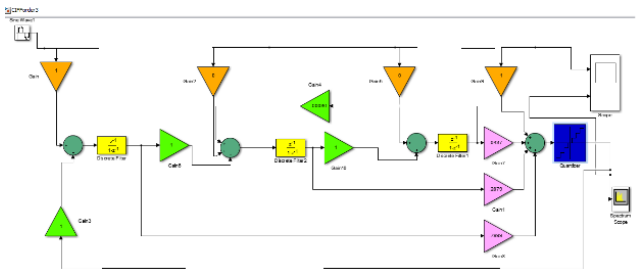

Fig. 8. The system level CIFF architecture of the Third-order Sigma Delta ADC

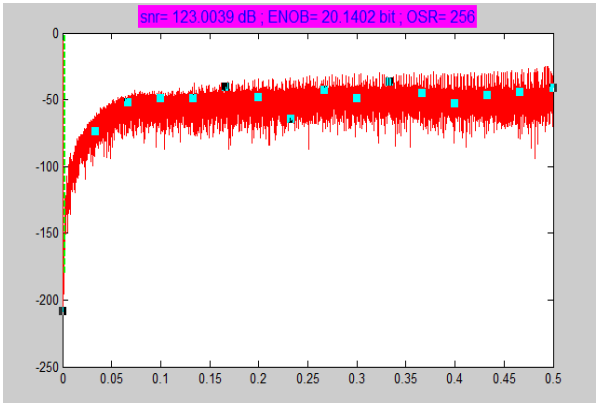

Fig. 9. The FFT spectrum of Single-bit quantization third order sigma-delta with considering OSR=256

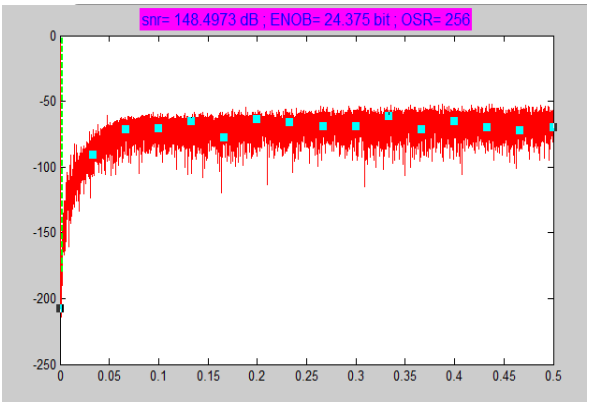

Fig. 10. The FFT spectrum of Multi-bit quantization third order sigma-delta with considering OSR=256

IV. System Level Model Simulation of MASH 1-1 (Two Stage) MASH 1-1-1 (Three Stage) MASH 2-1 (Two Stage) of the Sigma Delta ADC using MATLAB

Basically, the system level model MASH 1-1 (Two Stage) structure of the Sigma Delta ADC modulator is indicated in Fig. 11. The output FFT spectrum of the modulator is shown in Fig. 12 while both of the quantizer bits are considered the single one, and in Fig. 13 the first quantizer bit is supposed to be single and the second quantizer bit is chosen multi, meanwhile, in both of the cases the OSR=128, reliably. As simulation results prove that, in the second case (when first quantizer bit single and second quantizer bit multi) the SNR and Effective Number of Bits (ENOB) are better compared to the first case, as well.

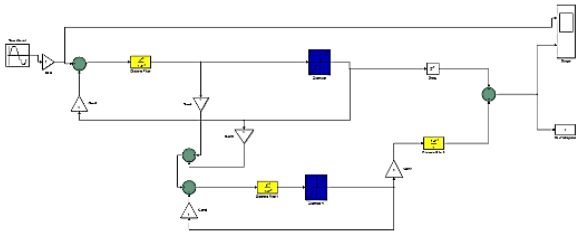

Fig. 11. The System level model MASH 1-1 (Two stage) structure of the Sigma Delta ADC

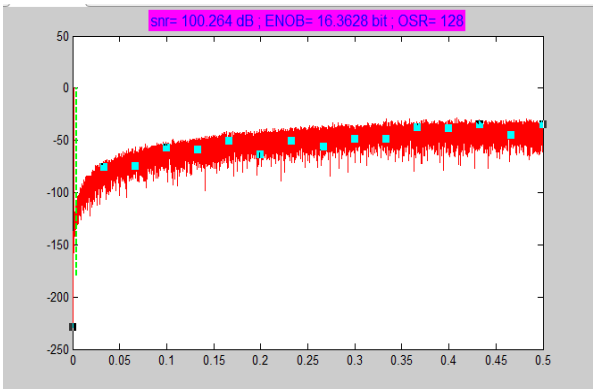

Fig. 12. The FFT spectrum of the MASH 1-1 structure when both of the quantizer bits are chosen single with considering OSR=128

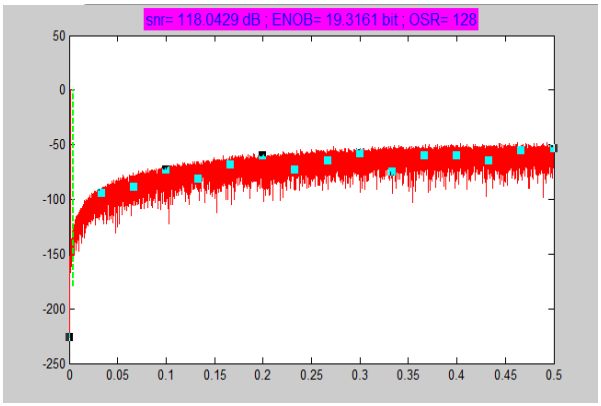

Fig. 13. The FFT spectrum of the MASH 1-1 structure when first quantizer bit single and second quantizer bit multi with considering OSR=128

The system level model MASH 1-1-1 (Three Stage) structure of the Sigma Delta ADC is indicated in Fig. 14. The output FFT spectrum of the modulator is shown in Fig. 15 while all of the three quantizer bits are considered the single bit, and in Fig. 16 the first and second quantizer bits are supposed to be single, and the third quantizer bit is chosen multi. Also, in Fig. 17 the first quantizer bit is considered to be single, and the second and third quantizer bits are selected multi. Fig. 18 shows the FFT spectrum when the first quantizer bit is supposed to multi, and the second and third quantizer bits are nominated single and finally, in Fig. 19 the first and third quantizer bits are designated to be single, and the second quantizer bit is chosen multi, as well. Meanwhile, in all of the cases the OSR=128, constantly. As simulation results prove that,

when first quantizer bit is considered to be single, and the second and third quantizer bits are selected multi, in this case the SNR and the ENOB are maximum value, also, when the first quantizer bit is supposed to multi, and the second and third quantizer bits are nominated single, in this case, the SNR and the ENOB are minimum value, noticeably.

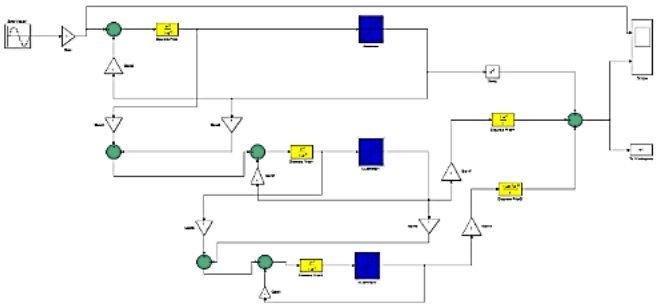

Fig. 14. The System level model MASH 1-1-1 (Three stage) structure of the Sigma Delta ADC

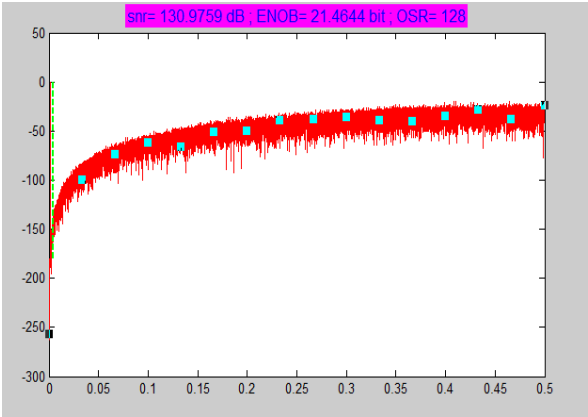

Fig. 15. The FFT spectrum while all of the three quantizer bits are considered the single with considering OSR=128

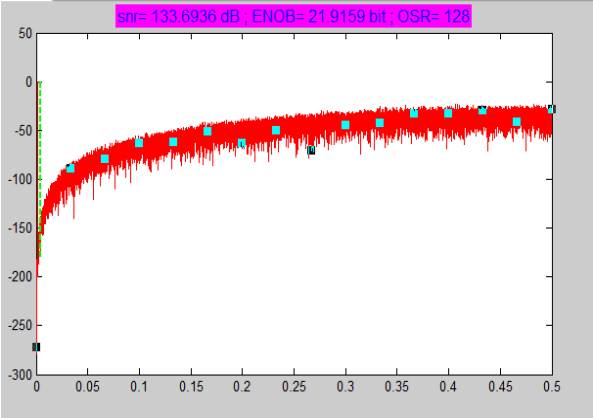

Fig. 16. The FFT spectrum while the first and second quantizer bits are single and the third quantizer bit is multi with considering OSR=128

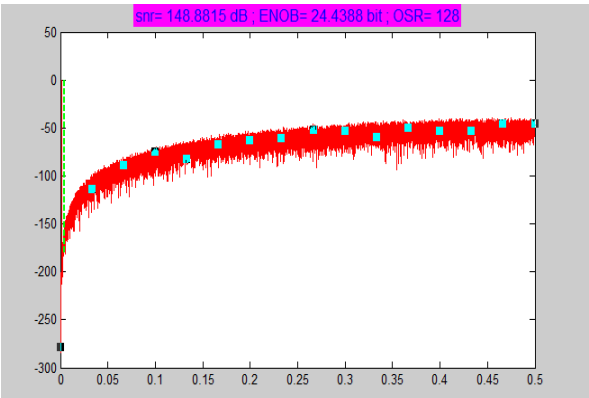

Fig. 17. The FFT spectrum while the first quantizer bit is single and the second and third quantizer bits are multi with considering OSR=128

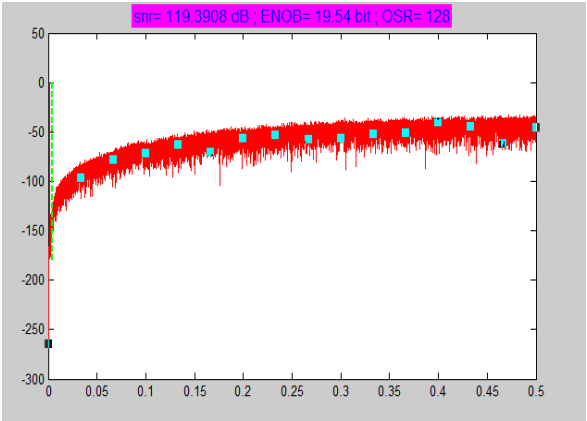

Fig. 18. The FFT spectrum when the first quantizer bit is multi and the second and third quantizer bits are single with considering OSR=128

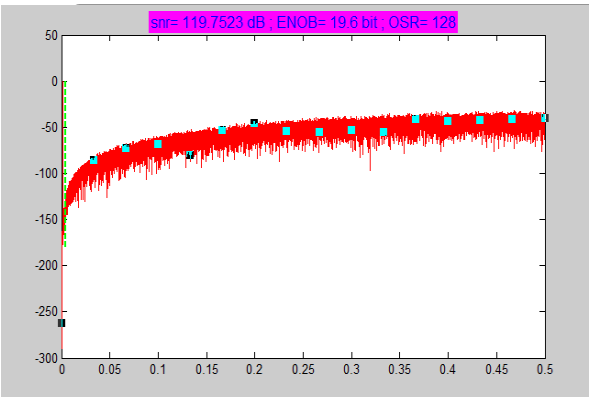

Fig. 19. The FFT spectrum while the first and third quantizer bits are single and the second quantizer bit is multi with considering OSR=128

The system level model MASH 2-1 (Two Stage) structure of the Sigma Delta ADC is indicated in Fig. 20. The output FFT spectrum of the modulator is shown in Fig. 21 while both of the quantizer bits are

considered the single one, and in Fig. 22 the first quantizer bit is supposed to be single and the second quantizer bit is chosen multi. Also, in Fig. 23 the first quantizer bit is considered to multi and the second quantizer bit is selected to be single. In the meantime, in both of the cases the OSR=128, consistently. As simulation results prove that, when first quantizer bit is considered to be single, and the second quantizer bit is designated multi, in this case the SNR and the ENOB are maximum value, also, when the first quantizer bit is supposed to multi and the second quantizer bit is nominated single, in this case, the SNR and the ENOB are minimum value, conspicuously.

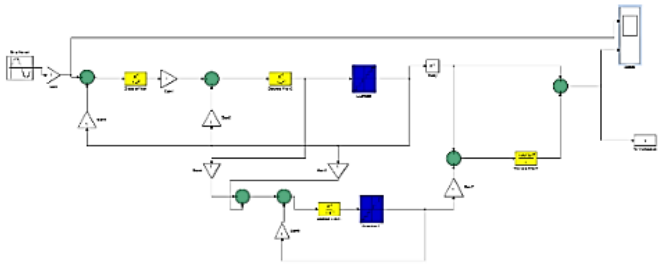

Fig. 20. The system level model MASH 2-1 (Two Stage) structure of the Sigma Delta ADC

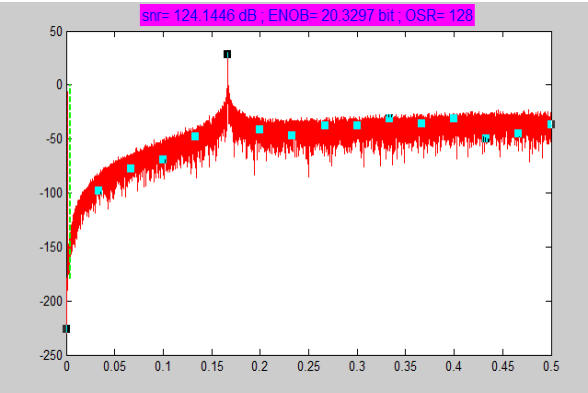

Fig. 21. The FFT spectrum while both of the quantizer bits are the single with considering OSR=128

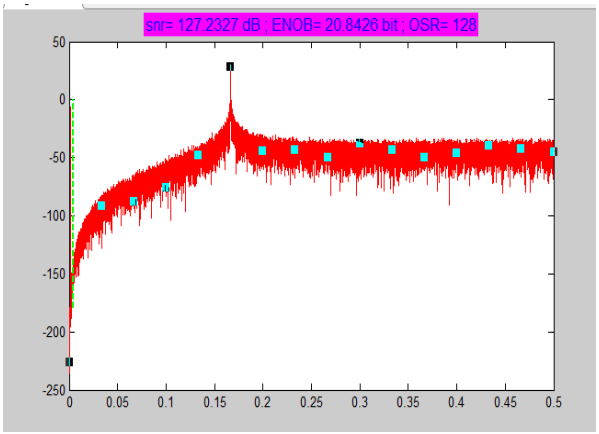

Fig. 22. The FFT spectrum while the first quantizer bit is single and the second quantizer bit is multi with considering OSR=128

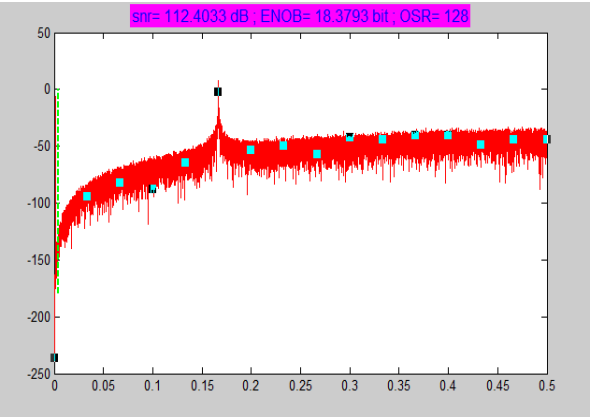

Fig. 23. The FFT spectrum while the first quantizer bit is multi and the second quantizer bit is single with considering OSR=128

V. Simulation Results

In this section, the comparison table of the different types of the sigma-delta modulator are presented. Tabel I and II are the comparison tables for the CIFF structure with considering OSR=128 and OSR=256 respectively. Also, the simulation results of the MASH 1-1, MASH 2-1 and MASH 1-1-1 structures are presented in different cases in Tables III, IV and V, respectively. As simulation results prove that, the first order CIFB structure has minimum SNR and MASH 1-1-1 structure with good optimization has the maximum SNR, respectively. The simulation results of the paper are performed using the MATLAB software.

TABLE I. OSR 128

SIMULATION	**CIFF**					
ORDER	1	1	2	2	3	3
OSR	128	128	128	128	128	128
Q*(bit)	1	4	1	4	1	4
SNR(dB)	48.97	70.96	71.9	100.73	91.49	120.5
ENOB (bit)	7.8	11.49	11.65	16.44	14.9	17.2

* Quantizer bit

TABLE II. OSR 256

SIMULATION	**CIFF**					
ORDER	1	1	2	2	3	3
OSR	256	256	256	256	256	256
Q(bit)	1	4	1	4	1	4
SNR(dB)	62.79	83.62	93.76	119.59	123	148.49
ENOB (bit)	10.13	13.52	15.28	19.57	20.13	24.37

TABLE III. MASH 1-1

SIMULATION	OSR	Q1 (bit)	Q2 (bit)	SNR (dB)	ENOB (bit)
MASH 1-1	64	1	1	85.47	13.9
MASH 1-1	64	1	4	103.9	16.97
MASH 1-1	64	4	1	71.9	11.65
MASH 1-1	128	1	1	100.26	16.6
MASH 1-1	128	1	4	118	19.3
MASH 1-1	128	4	1	85.67	13.94

TABLE IV. MASH 2-1

SIMULATION	OSR	Q1 (bit)	Q2 (bit)	SNR (dB)	ENOB (bit)
MASH 2-1	64	1	1	104.3	17
MASH 2-1	64	1	4	106.97	17.45
MASH 2-1	64	4	1	94.14	15.51
MASH 2-1	128	1	1	124.14	20.3
MASH 2-1	128	1	4	127.2	20.84
MASH 2-1	128	4	1	112.4	18.37

TABLE V. MASH 1-1-1

SIMULATION	OSR	Q1 (bit)	Q2 (bit)	Q3 (bit)	SNR (dB)	ENOB (bit)
MASH 1-1-1	64	1	1	1	110	18
MASH 1-1-1	64	1	1	4	113.9	18.5
MASH 1-1-1	64	1	4	4	128.1	21
MASH 1-1-1	64	4	1	1	99.8	16.29
MASH 1-1-1	64	1	4	1	100.9	16.49
MASH 1-1-1	128	1	1	1	130.97	21.46
MASH 1-1-1	128	1	1	4	133.69	21.9
MASH 1-1-1	128	1	4	4	148.8	24.43
MASH 1-1-1	128	4	1	1	119.3	19.54
MASH 1-1-1	128	1	4	1	119.7	19.6
MASH 1-1-1	256	1	1	1	154.1	24.98
MASH 1-1-1	256	1	1	4	154.2	25.2

Conclusion

In this paper, the Signal to Noise Ratio (SNR) parameter of the different types of the Sigma Delta ADC Modulators are studied and discussed, comprehensively. The CIFF structure of first, second and third orders with considering the different OSR are presented. Meanwhile, the MASH 1-1, MASH 2-1, and MASH 1-1-1 structures are analyzed and simulated, carefully, too. It is noteworthy that, as simulation results prove, the SNR and ENOB of each modulator is dependent on the value of the Order, OSR, and Quantizer bit parameters, extremely. For this case, in the design of the sigma-delta modulator, the designers must be considered and selected the suitable value for the mentioned parameters, carefully. Also, among of the presented modulators in this paper, the first order CIFB structure has minimum SNR and MASH 1-1-1 structure with good optimization has the maximum SNR, respectively. Finally, also, the simulation results of the MASH 1-1, MASH 2-1 and MASH 1-1-1 structures are presented in different cases in Tables III, IV and V, respectively. Simulation results of the proposed paper are simulated using the MATLAB software.

References

[1] S.Tao, A. Rusu, "A Power-Efficient Continuous-Time Incremental Sigma-Delta ADC for Neural Recording Systems", IEEE Transactions on Circuits and Systems,Vol. 62, no. 6, June 2015, pp: 1489 – 1498.

[2] Jnnuna G, S. Yellampalil, Swetha S, "Design and Implementation of Telescopic OTA in 8 Bit Second-Order Continuous-Time Band-Pass Sigma-Delta ADC", IEEE International Conference on Electronics, Communication and Computational Engineering, ICECCE 2014, pp: 1-7.

[3] M. Joseph, S. Sreelal, J. J. Edathala, "End to end simulation of sigma delta ADC", IEEE Annual International Conference on Emerging Research Areas and International Conference on Microelectronics, Communications and Renewable Energy, AICERA/ICMiCR 2013, pp: 1-4.

[4] N. N. Hurrah, Z. Jan, A. Bhardwaj, S. A. Parah, A. K. Pandit, "Oversampled Sigma Delta ADC decimation filter: Design techniques, challenges, tradeoffs and optimization", IEEE 2nd International Conference on Recent Advances in Engineering & Computational Sciences, RAECS 2015, pp: 1-6.

[5] A. Khurana, A. K. Sahu, A. Tiwari, "Design of low power VCO enabled quantizer in Continuous Time Sigma Delta ADC for signal processing application", IEEE International Conference on Wireless Communications, Signal Processing and Networking ,WiSPNET 2016, pp: 2113–2117.

[6] H. Molaei, A. Khorami, M. S. E. Sendi, K. Hajsadeghi, "A four bit low power 165MS/s flash-SAR ADC for sigma-delta ADC application", IEEE International Conference on Electronics, Circuits and Systems , ICECS 2015, pp: 153–156.

[7] R. LAHOULI, M. B. ROMDHANE, C. REBAI, D. DALLET, "Digital Reconstruction Stage of Parallel FBD Sigma Delta ADC.

[8] R. Kostack, A. Naeini, H. Stockinger, A. Brönner, F. Ellinger, "A direct RF sampling receiver using continuous-time band-pass sigma-delta ADC with active inductor in CMOS", IEEE MTT-S Latin America Microwave Conference, LAMC 2016, pp: 1–4.

[9] Y. Tembhre, A. K. Sahu,"Testing of an 8-bit Sigma Delta ADC Based on Code Width Technique Using 45nm Technology", IEEE International Conference on Micro-Electronics and Telecommunication Engineering , ICMETE 2016, pp: 416–420.

[10] H. Deng, Z. Wang, "A Chopper-Stabilized Amplifier for Input Signal Amplification of Sigma-delta ADC", IEEE International Conference on Anti-Counterfeiting, Security and Identification, ASID 2014, pp: 1-4.

[11] S. Mahdavi, E. Ghadimi, "A New 13-bit 100MS/s Full Differential Successive Approximation Register Analog to Digital Converter (SAR ADC) Using a Novel Compound R-2R/C Structure", 2017 IEEE 4th International Conference on Knowledge-Based Engineering and Innovation (KBEI), 2017, pp: 0237 - 0242.

[12] J. Cao, Y. Liu, B. Jiang, X. Liu, "The Design and Implementation of Sigma Delta ADC Digital Decimation Filter", IEEE International Conference on Information Science and Cloud Computing Companion, ISCC-C 2013, pp: 335-338.

[13] S. Mahdavi, F. Noruzpur, R. Ebrahimi, Z. Alizad "Analysis Simulation and Comparison Different Types of the Sigma Delta ADC Modulators Based on Ideal Model System Level and behavioral Model Using MATLAB", 2017 IEEE 4th International Conference on Knowledge-Based Engineering and Innovation (KBEI), 2017, pp: 0252 – 0259.

[14] M. Barangi, A. Beirami, H. Nejati, and W. H. Ali, "A Continuous-Time Sigma-Delta ADC with Tunable Pass-Band for Multi-Standard Applications", IEEE 56th International Midwest Symposium on Circuits and Systems, MWSCAS2013, pp: 633-636.

[15] S. Mahdavi, T. Torabi Ghaznag "A 2.52 fJ/Conversion-Step 12-bit 154MS/s with 68.78dB SNDR Full Differential SAR ADC with a Novel Capacitor Switching Scheme", 2018 26th Iranian Conference on Electrical Engineering (ICEE2018), 2018, pp: 81 - 86.

[16] P. Trivedi, A. Verma, P. Tripathi, "Characterization and Optimization of Sigma-Delta ADC", IEEE Third Asian Himalayas International Conference on Internet, AHICI 2012, pp: 1-5.

[17] H. V. Palagiri, M. L. Makkena, K. R. Chantigari, "Performance Analysis of First Order Digital Sigma Delta ADC", IEEE Fourth International Conference on Computational Intelligence, Communication Systems and Networks, CICSyN 2012, pp: 435-440.

[18] L. Zhao, C. Deng , H. Chen, G. Wang, Y. Cheng, " A 1-V 23-µW 88-dB DR Sigma Delta ADC for High-Accuracy and Low-Power Applications", IEEE 11th International Conference on ASIC, ASICON 2015, pp: 1-4.

[19] Q. Yu, K. Wang, X. Cao, Y. Wang, T. Yi, B. Lu, Y. Chen, Zh. Hong, " A 4-channel ASIC for X-ray CCD Readout Based on Incremental Sigma Delta ADC", IEEE 13th International Conference on Solid-State and Integrated Circuit Technology, ICSICT 2016, pp:106–108.

[20] Sh.Tao, A. Rusu, " A Power-Efficient Continuous-Time Incremental Sigma-Delta ADC for Neural Recording Systems", IEEE Transactions on Circuits and Systems I, 2015, Vo: 62, Issue: 6, pp: 1489–1498.

[21] S. Mahdavi, "A 12 bit 76MS/s SAR ADC with a Capacitor Merged Technique in 0.18µm CMOS Technology", Journal of Electrical and Computer Engineering Innovations (JECEI), 2017, vol.5, issue.2, pp. 121-130.

[22] N. N. Hurrah, Z. Jan, A. Bhardwaj,Sh. A. Parah, A. K. Pandit, " Oversampled Sigma Delta ADC Decimation Filter: Design Techniques, Challenges, Tradeoffs and Optimization" , 2015 2nd International Conference on , RAECS 2015, pp: 1 – 6.

[23] S. K. Mankani, Sh. Sajjanar, Mohana, H. V. R.Aradhya, "Power and Area Optimization of Decimation Filter for Application in Sigma Delta ADC" , International Conference on Circuits, Controls, Communications and Computing (I4C)2016, pp: 1–5.

[24] Y. Tembhre, A. K. Sahu, "TESTING OF AN 8-BIT SIGMA DELTA ADC BASED ON CODE WIDTH TECHNIQUE USING45nm TECHNOLOGY", ICMETE 2016, pp: 416–420.

[25] V. Zhmud, L. Dimitrov, A. Taichenachev, "The Use of Sigma-Delta-ADC in the Commutation mode", SIBCON 2017, pp: 1–4.

[26] S. Mahdavi, M. Poreh, L. Alizadeh, B. Moradkhani, R. Ebrahimi "A 1.25GS/s 12bit and 2.27mW Digital to Analog Converter (DAC) With 70.22 SNDR Based on New Hybrid R-C Procedure in 180nm CMOS", International Journal of Microelectronics and Computer Science, Poland, Vol.8, No.4, pp.127-132.

[27] S. Mahdavi, K. Hadidi "A 14 bit 17 MS/s 80dB SNDR Low Power SAR ADC with Energy-Efficient Switching Procedure", unpublished.

[28] S. Mahdavi, R. Ebrahimi, A. Daneshdoust, A. Ebrahimi, "A 12bit 800MS/s and 1.37mW Digital to Analog Converter (DAC) Based on Novel R-C Technique," 2017 IEEE International Conference on Power, Control, Signals and Instrumentation Engineering (ICPCSI), 2017, pp: 163 – 166.

[29] P. A. HarshaVardhini, "Analysis of Integrator for Continuous Time Digital Sigma Delta ADC on Xilinx FPGA", ICEEOT 2016, pp: 2689–2693.

[30] Y. Shaojun, T. Ziquan, J. Yueming, D. Naiying, "The Design of a Multi-bit Sigma-delta ADC Modulator", IEEE 2nd International Conference on Measurement, Information and Control, MIC 2013, vol. 01, pp: 280-283.

[31] J. R. Custódio, J. Goes, N. Paulino, J. P. Oliveira, and E. Bruun, "A 1.2-V 165- W 0.29-mm Multibit Sigma-Delta ADC for Hearing Aids Using Nonlinear DACs and With Over 91 dB Dynamic-Range", IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, VOL. 7, NO. 3, JUNE 2013, pp: 376–385.

[32] K. L. Krishna, T. Ramashri , D. Reena, "A 1V Second Order Delta Sigma ADC in 130nm CMOS", IEEE International Conference on Information Communication and Embedded Systems, ICICES 2014, pp: 1-5.