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Design of a High Performance Reversible Combinational Digital circuit based on a new Reversible Gate in QCA Technology

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***Abstract*— Quantum-dot Cellular Automata (QCA) technology and Reversible logic are presented to overcome the various problems such as the chip size reduction and power consumption in the traditional CMOS designs. In this paper, QCA is considered as a professional method for implementation of the reversible logic. Firstly, a new block of two-input XOR gate is provided, and then the novel universal reversible gate is designed based on this block. Using this reversible structure, we can design useful QCA combinational digital circuits. Hence, we design a one-bit full adder using new reversible gate, this structure has single layer and coplanar (clock based) cross-wiring. The proposed reversible full adder achieves 63.83% and 55.38% in the number of cells and occupied area, respectively with Compared to previous best designs. The latency in our proposed structure is 1 clock cycle, the operation of the proposed structures has been tested with QCA Designer version 2. 0. 3.**

Keywords — Reversible logic, Quantum-dot Cellular Automata (QCA), XOR gate, Full adder.

I. INTRODUCTION

ECENT researchs have shown that traditional CMOS technology has encountered problems such as leakage current and high power dissipation [1]. QCA technology is a good substitution to CMOS technology with useful aspects such as delay, power dissipation and occupied area. Quantum-dot cellular automata technology as first introduced in 1994. In QCA cells, values of 0 and 1 are created as special shapes of quantum dots. All cells have a square shape that quantum dots are placed in square corners. Any cell has two additional electrons arranged in the form of a diagonal across cell, condition of the cell polarization determines the values of zero and one cell. In this technology, since no electricity is generated between the cells, the power consumption is very low [2-6].

In the irreversible digital circuit, the input information is eliminated because this information is not recovered from the output data, hence reversible logic most commonly used in the quantum computing. In 1961, R. Landauer showed that the energy loss to lose any bit of data in irreversible logic is K.T.ln2 joules, Where K is equal 1.38×10^{-23} JK^{-1} (Boltzmann's constant) and T is environment absolute temperature [7]. Bennet's theory in 1973 proved if the circuit contains only of reversible gates, this amount does not occur from energy dissipation [8]. A reversible gate has an N-input and N-output that provides a one-to-one relationship between the input and output vectors, so the input data can be retrieved from the output data. Several designs of reversible schemes have been reported in other works, various examples are presented in papers [9-15]. In [16], the author implemented the new efficient reversible Feynman, Double Feynman, Fredkin, Peres, Toffoli and R Gates. Also, the structures of three bit binary to Gray converter and four bit parity checker designed with reversible gates. All structures have the minimum cell count, latency and occupied area without any crossover. In [17], the authors introduced a new synthesis method for several reversible gates such as Toffoli, Fredkin. Also, they presented a new method for designing proposed reversible structures in QCA technology. The results showed that all circuits have high efficiency performance and the lowest number of garbage outputs and majority gates. In [18], the authors suggested a new plan of XOR gate in QCA technology. They didn't used majority gates and rotated cells, hence reported structures have superiorities in comparison with other designs in terms of number of cells, latency, power consumption and area. In [19], the authors presented a checker and parity bit generator circuits for nano-communication applications. In all circuit improved principle parameters like as occupied area, power consumption, circuit complexity and delay. In [20], the authors presented a new design of 3×3 reversible gate. For performance analysis of this structure, a design of one bit reversible full adder evaluated based on coplanar QCA technology. The simulation results indicated that proposed reversible full adder has significantly improved in various metrics such as complexity, area, delay. In [21], the authors presented a new design of two-input XOR gate based on QCA technology. This gate was improved in terms of complexity and delay. In [22], the authors evaluated the various digital circuits in QCA technology. They achieved a significant reduction of the number of cells and occupied area in QCA layout. In [9], the authors offer a new reversible gate which has a parity

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preserving property in QCA technology, the proposed design succeed in getting to enhancement 62.5% and 23.07% of the number of cells and occupied area in checking with previous works. In [10], QCA has been examined as a method of implementation to design a novel universal reversible logic. Then, by using a new XOR gate, a new approach is proposed for implementing 2:1 multiplexer. This gate with a reduction of 24% achieves the lowest cost in comparison to the other designs that presented so far. In order to utilize the ability of reversibility property in reversible structures, the proposed reversible gate is being used to design all basic flip flops (D, T, SR and JK flip flops). In [11] A new structure of fault tolerant reversible full adder gate. Is presented, the proposed design is evaluated with other available ALU designs and is efficient in design parameters such as complexity and quantum cost. In [23] five parity preserving reversible multiplier circuits have been designed, the simulation results indicated the superiority of all designs in comparison with existing designs, according to the reversible logic principal definitions mainly the quantum cost and number of gates. In [13], the authors provide various designs of reversible gates include Fredkin, Feynman, Peres and Toffoli, gates with QCA cells. These primary gates are used generally in designing large reversible circuits. All designs are measured in terms of power consumption and hardware complexity. In [24], structural examples and power examination of five input majority gates are shown. To assess the importance of reported gate, they presented a new reversible full adder circuit. The proposed full adder has single layer cross wiring, this circuit is robust and high performance, in this design is obtained 20% progression in the number of cells and occupied area has reduced 7% in comparison with other designs. In [25], the authors improved reversible full adder based on QCA technology. This circuit reduces the cell count in comparison with the different full adders. As well as, the delay has retained at least value. For design this circuit, a various formulas have been defined to carry and sum outputs. Finally, this QCA-based reversible full adder is designed to create various types of ripple carry adders. In [26], the authors designed a great scheme of three input XOR gate. This XOR gate is used to design a 2-4 compressor with aim to reduce the number of gates and complexity of the proposed circuit. In [27], A new QCA layout of the XOR gate with two inputs is introduced that is used to design a one bit reversible full adder. The main advantage of this gate is that it only requires 10 QCA cells for implementation. In [28], a coplanar QCA architecture has been used in the design of full adders in QCA technology that reduce the QCA cells and occupied area. Also, the latency of these circuits is zero. In this paper, all circuits get better 23% in QCA cells and 48% in required space by comparing the best of the previous designs. In [29], a novel QCA one-bit comparator presented. The reported design showed an improvement in the main parameters like cell counts and time delay in comparison with the best previous one-bit comparator, for design this structure obtained 10% reduction in cell counts, also latency was 1.25 clock cycles.

In this research, we introduce a new 3*3 reversible gate using QCA technology, this gate can perform as a universal gate and the effectiveness of this gate is evaluated through the realization of 13 standard combinational logic functions. The main work in our investigate is given a new model for reversible digital circuits such as a one bit full adder using two input XOR gate without any cross wiring. QCA exhibition of the proposed structures has been done with QCA Designer version 2. 0. 3.

The remains of the paper are formed as the following. In part 2, the background of QCA basic explanations and reversible logic are expressed. Design a new XOR gate is offered in part 3. Part 4 describes the proposed reversible gate and realizing standard functions using this gate. In part 5, a design of novel structures such as a one-bit full adder based on the proposed reversible gate is provided, simulation results and comparison with previous papers are investigated in part 6. At the end, the conclusion is given in part 7.

II. BACKGROUND OF RESEARCH

A. *Fundamental concepts of QCA technology*

QCA cells are the main unit of QCA layout structures. According to Figure 1 (a), each QCA cell contains of 4 quantum dots and 2 electrons in these locations. All electrons can tunnel between neighbor dots, while these electrons can't tunnel to the outside of this cell. The position of these electrons creates two different forms of polarization, namely P = +1 to indicate logic "1" and P = -1 to indicate logic "0". The basic blocks of the QCA circuits are inverter gate and majority gate. The two different forms of inverters are presented in Figure 1 (b, c). The logic equation of majority function is equivalent $M(A,B,C) = AB + BC + AC$ and according to Figure 1 (d), this gate consists of 5 QCA cells. Also, using the majority gate, the AND gate and the OR gate can be obtained by setting its inputs at P = -1 or P = +1, respectively.

Given that synchronization is an important subject in the QCA circuits design, the time zone segmentation is utilized to control the direction of the flow of circuit signals and provide the demanded power for operating in the QCA circuits [30]. As illustrated in Figure 2, the clocking used in QCA circuits consists of four steps: Relax, Release, Switch and Hold. Within switch stage, the Barriers between dots slowly expansion and the electrons are pulled to the corner points. In this phase, the electrons focus on the status of the input cells. In the hold period, the barriers of inter-dots are raised to high levels and the position of the electrons stays constant, this cell is used as an input cell for other cells in the next clock zone. During the release stage, the barriers are reduced. Finally, in relax stage, all barriers are maintained in a low state and none of the cells do not have polarization. Generally, there are three various shapes of wire-crossing in QCA technology: (a) Coplanar (rotated cells), (b) Multilayer wire-crossing and (c) Coplanar (clocking based). Figure 3 shows different cell layouts of wire- crossing in QCA technology.

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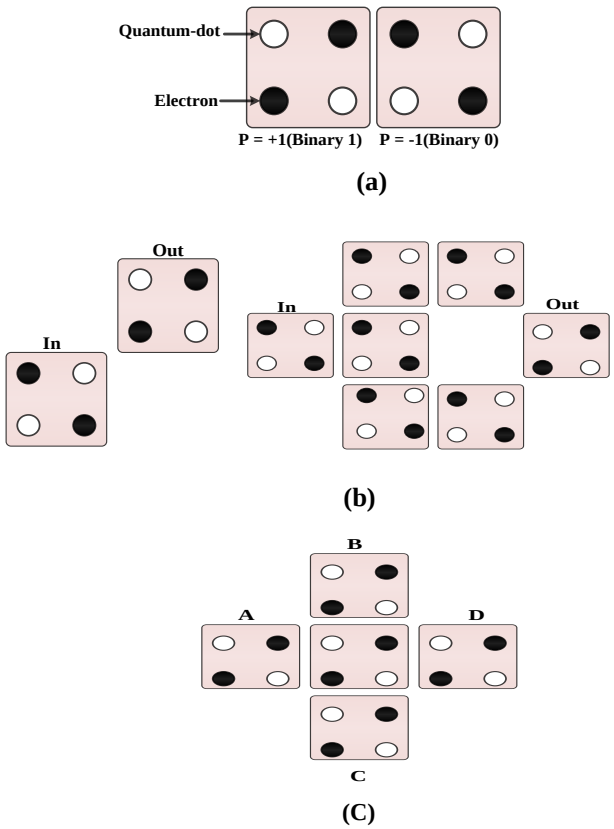

Fig. 1. Main QCA structures (a) QCA cell, (b) Different type of Inverter gate, (c) 3-input majority gate.

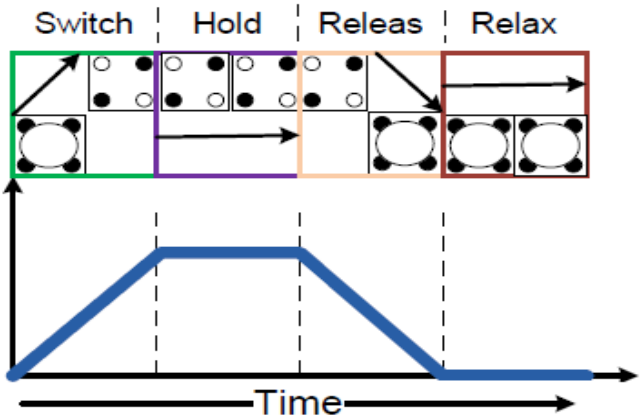

Fig. 2. QCA clocking with different phases [31].

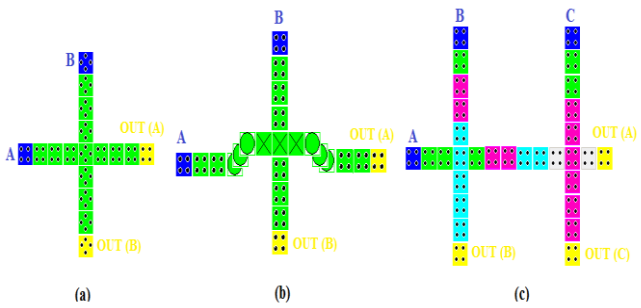

Fig. 3. Different methods of wire-crossing: (a) Coplanar rotated cells, (b) Multilayer, (c) Coplanar clocking based [32].

2. Reversible Logic

If there is an identical relationship between the input vector and the output vector, a logic gate is reversible. Each individual output vector is determined from the input vector and each input vector is individually regained from the output vector. A reversible gate is defined by N × N, give this meaning that the number of inputs is N and is equal to the number of outputs [33]. The constant inputs are the inputs whose values are kept fixed at 0 or 1 to create a specified logical function. In other hand, this zero and one input are added to a gate in order that can make its reversible structure. In addition, there are outputs which called garbage outputs and not used in any calculation. The quantum cost is defined by the total number of primary gates for explanation the major function [34]. Some of the most important introduced gates in reversible logic:

- **NOT Gate**

The NOT gate is the simplest reversible gate, a 1×1 reversible gate with a quantum cost of zero [35].

- **Feynman Gate**

The Feynman Gate is a 2×2 gate which recognized as uncontrolled (C-NOT) gate, The inputs are (A, B) and the outputs are $P = A$ and $Q = A \oplus B$. This gate has a quantum cost of one [35].

- **Fredkin gate**

The Fredkin gate is a 3×3 gate, the vector of input is $I(A, B, C)$ and the output vector of this gate is $O(P, Q, R)$. The outputs function are denoted by $P = A$, $Q = \overline{A}B \oplus AC$ and $R = \overline{A}C \oplus AB$. In the design of this gate, the Quantum cost value should be five [35].

- **Toffoli Gate**

The Toffoli gate is a 3×3 reversible gate. The input vector is denoted a $I(A, B, C)$ and the output vector is indicated $O(P, Q, R)$. The logical function of outputs is described by $P = A$, $Q = B$ and $R = AB \oplus C$. The value of Quantum cost is equal five [35].

- **Peres Gate**

The Peres gate has three input and three output, this gate called 3×3 reversible gate. The input vector is exhibited $I(A, B, C)$ and the output vector is shown $O(P, Q, R)$. The outputs are designated by $P = A$, $Q = A \oplus B$ and $R = AB \oplus C$. Quantum cost of this gate is four [35].

III. The Proposed Improved XOR Gate

XOR (Exclusive – OR) is a universal logic gate and has extensively applied in digital circuits. This gate is utilized in various types of digital circuits like as multiplexers, full adders, comparators, arithmetic and logic unit, reversible logic circuits and so on. In practice, this gate require to 2 inputs (A, B) and one output (F), which performs this logic

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operation: $F = \bar{A}B + A\bar{B}$. Because of extensive use of this gate several different shapes of QCA layout have been offered so far [10, 36-39]. These XOR gates have different QCA cells, occupied area and clock zone. As presented in paper [40], a QCA XOR gate have designed that include 14 cells, 0.01 μm^2 area and 0.5 clock cycles for delay. Therefore, at present work, we have improved this structure by using less QCA cell and less occupied area, the QCA layout of the proposed gate is illustrated in Figure 4. The comparison of these structures is shown in Table 1. In the rest of this work, we use of this improved XOR gate for designing different circuits.

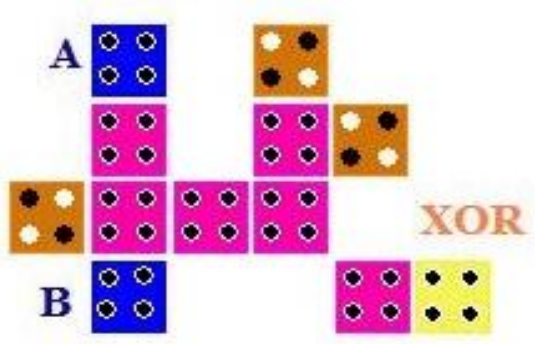

Fig. 4. QCA layout of the improved proposed XOR structure.

TABLE I
COMPARISON OF THE VARIOUS XOR GATES

QCA XOR design	Number of Cells	Occupied Area (μm^2)	Delay (Clock phase)	Type of crossover
Presented in [37]	85	0.078	1.25	None
Presented in [39]	28	0.02	0.75	None
Presented in [36]	12	0.011	0.5	None
Presented in [38]	10	0.008	1	Coplanar
Presented in [10]	14	0.01	0.5	None
Proposed Improved XOR gate	12	0.008	0.5	None

IV. THE INTRODUCTION OF A QCA REVERSIBLE GATE

In this section a new QCA implementation of a 3×3 reversible gate is introduced. According to the truth Table (Table 2), this gate can make a one to one relationship between input and output signals, and also the number of inputs is same with the number of outputs so this structure is a reversible gate. The logical relation among all inputs and outputs express as $P = M(A,B,C), Q = \bar{A}B \oplus C, R = (A \oplus B)^-$, the block diagram of the new reversible gate is illustrated in Figure 5.

TABLE II
DISPLAY THE TRUTH TABLE OF THE PROPOSED REVERSIBLE GATE

A	B	C	P	Q	R
0	0	0	0	0	1
0	0	1	0	1	1
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

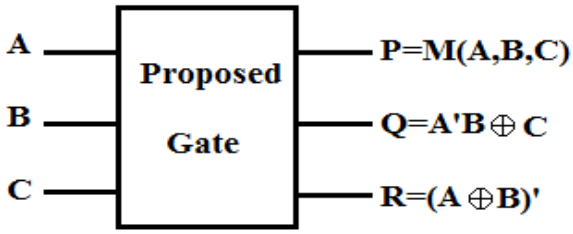

Fig. 5. Schematic of the proposed reversible gate Block diagram.

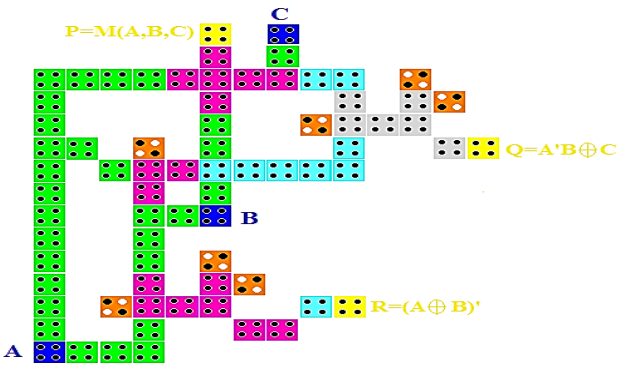

Fig. 6. QCA implementation of the new 3×3 reversible gate.

B. The proposed Reversible Gate as a Universal Structure

A universal logic gate is a logic gate that can build all the seven basic Boolean functions (NOT, AND, NAND, OR, NOR, Ex-OR, Ex-NOR) [41]. According to Table 3, the proposed reversible gate is a universal because all the basic logic functions can be implemented by using the various inputs of this gate.

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TABLE III
IMPLEMENTATION OF THE BASIC BOOLEAN FUNCTIONS USING THE PROPOSED REVERSIBLE GATE

Logic operators	Arrangement of the required inputs
1. NOT	(A,1,0)
2. AND	(A, B, 0)
3. NAND	($\bar{A}$,$\bar{B}$,1)
4. OR	(A,B,1)
5. NOR	($\bar{A}$,$\bar{B}$,0)
6. Ex-OR	(0,A,B)
7. Ex-NOR	(A,B,C)

2. *Efficiency evaluation of 13 logical Standard Functions Using the Proposed Reversible Gate*

In this section, the proposed gate is compared to the previous works for the synthesis of logic design. Thirteen standard functions (shown in Table 4) can construct all 256 Boolean functions. These thirteen functions can be designed by the proposed gate as structures are given in Figure 7. In Table 4 the mean count of necessary gates for design these standard functions which are compared with other gates. The average count of gates for the proposed reversible gate is less than Toffoli, Fredkin and RUG gates, but its equal with RM gate. The comparative performance in the midst of the new reversible gate and the former designs is given in Table 9. In all designs, main criterion such as number of cells, occupied area, latency, type of cross-wiring and cost value, the cost function value in QCA based circuits can calculate according to equation (1) and relies on area, power and delay [10]. The paper [42] shows that the average value of power consumption per cell for the various full adder designs is approximately the same, which means that the power is equal to the complexity (gate count).

$$Cost = Area \times Delay \times Power \quad (1)$$

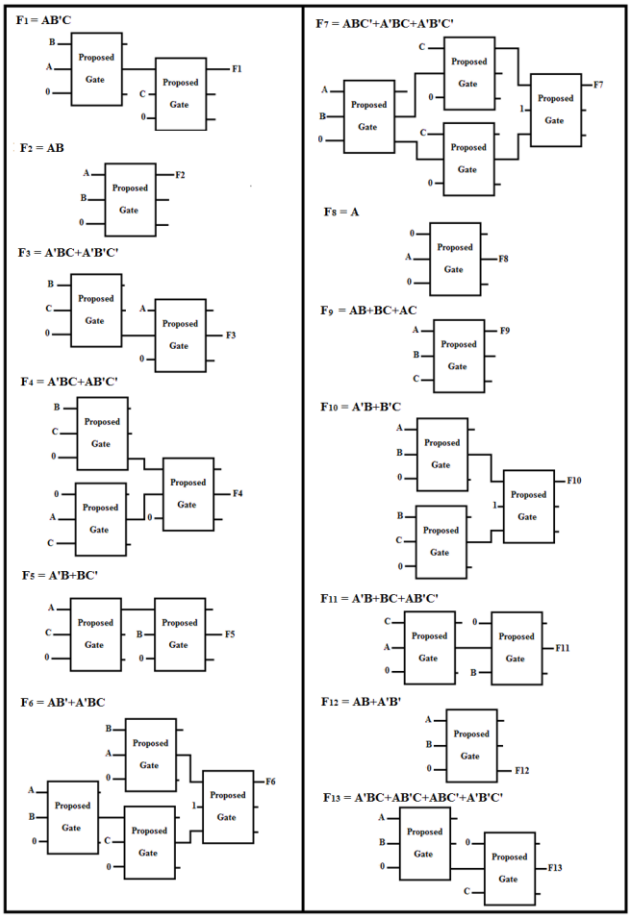

Fig. 7. Implementation of All 13 standard logical functions using the new proposed reversible gate.

TABLE IV
COMPARISON GATE COUNT OF THE 13 STANDARD LOGIC FUNCTIONS WITH VARIOUS REVERSIBLE STRUCTURES

Standard Function	Fredkin Gate in [48]	Toffoli Gate in [43]	Fredkin Gate in [43]	RUG Gate in [44]	RM Gate in [45]	NRG Gate in [10]	R-CQCA Gate in [46]	Proposed gate
1. AB'C	2	2	2	3	2	2	2	**2**
2. AB	1	1	1	1	1	1	1	**1**
3. A'BC+A'B'C'	3	3	3	2	2	3	3	**2**
4. A'BC+AB'C'	4	4	2	3	3	3	2	**3**
5. A'B+BC'	2	2	2	3	2	2	2	**2**
6. AB'+A'BC	5	3	2	3	2	2	3	**4**
7. ABC'+A'BC+A'B'C'	6	5	4	3	3	3	3	**4**
8. A	1	1	1	1	1	1	1	**1**
9. AB+BC+CA	5	4	4	1	5	2	3	**1**
10. A'B+B'C	1	3	1	3	1	2	1	**3**
11. A'B+BC+AB'C'	6	1	4	3	2	2	3	**2**
12. AB+A'B'	2	1	2	1	2	1	2	**1**
13. A'BC+AB'C+ABC'+A'B'C'	3	3	4	3	2	2	2	**2**
Total Number of Gates	41	33	31	30	28	26	28	**28**
The Average Number of Gates	3.1538	2.5834	2.3846	2.3077	2.1538	2	2.1538	**2.1538**

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3. AOP Analysis

In this section, we study the effect of temperature changes in the output polarization state of the proposed reversible gate. The average output polarization (AOP) at various temperatures is calculated by the coherence vector simulator engine in QCA Designer software. The value of the average output polarization is gently reduced with increasing temperature [47]. The AOP for an output cell at any specific temperature is determined by estimate the difference of the maximum and minimum of the polarization value and dividing it's by two. The AOP analysis for the outputs of proposed reversible gates at different rates of temperature (1-13k) is illustrated in Table 5.

TABLE V
AOP OF THE PROPOSED REVERSIBLE GATE AT DIFFERENT TEMPERATURE LEVELS

Output cell	AOP temperature												
	1	2	3	4	5	6	7	8	9	10	11	12	13
P	3.518	3.518	3.518	3.518	3.514	3.503	3.485	3.451	3.409	3.352	3.286	3.208	3.124
Q	3.494	3.494	3.494	3.494	3.486	3.474	3.442	3.398	3.328	3.238	3.122	2.984	2.8
R	3.496	3.496	3.496	3.494	3.488	3.474	3.444	3.4	3.337	3.249	3.142	3.008	2.848

V. INTRODUCING THE DESIGN OF A NEW REVERSIBLE FULL ADDER

In this section, to prove the importance of the proposed gate, one type of combinational digital circuits such as a reversible full adder is investigated using the new reversible gate.

1. The Proposed Reversible full adder

Full adder can perform as a one of the principal elements in the design of the various digital units. As shown in Figure 9, we use the proposed reversible gate which introduced in the previous section to design a one-bit reversible full adder. This circuit has 4 inputs and 4 outputs which the number of constant input is 1, also 2 of the outputs are garbage outputs (G1, G2). The Truth table for the proposed full adder is depicted in Table 6. Sum and carry outputs are the main outputs and expressed in the following:

$$SUM = A \oplus B \oplus C \tag{3}$$

$$CARRY = M(A,B,C) = AB + BC + AC \tag{4}$$

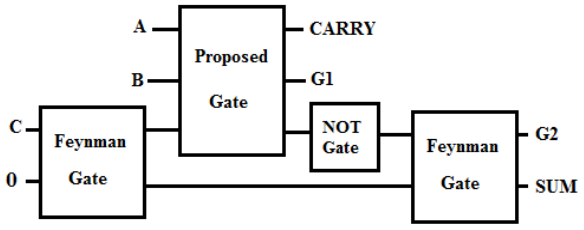

Fig. 9. Schematic of the proposed reversible full adder.

TABLE VI
TRUTH OF THE NEW 3×3 REVERSIBLE FULL ADDER

A	B	C	Sum	Carry	G1	G2
0	0	0	0	0	0	0
0	0	1	1	0	1	0
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	0	1
1	0	1	0	1	1	1
1	1	0	0	1	0	0
1	1	1	1	1	1	0

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As QCA cells implementation with the proposed one-bit reversible full adder structure illustrated in Figure 10. This circuit consists of different logic gates such as Four 2-input XOR gates, one OR gate, two AND gates and one NOT gate. The proposed QCA layout is designed with a one layer. This QCA reversible structure contains about 115 cells and 1 clock cycles. Besides, this structure occupies nearly 0.116μm^2.

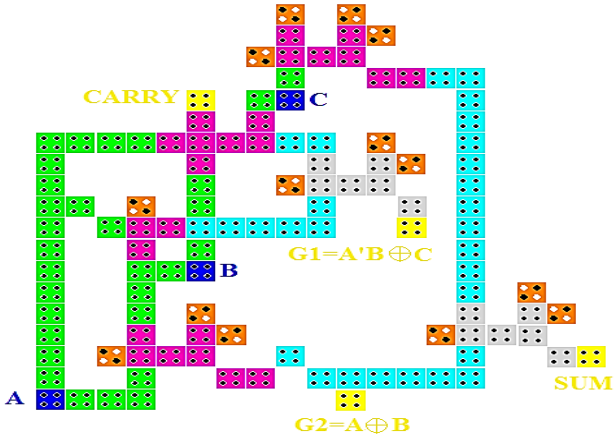

Fig. 10. Display of the QCA layout for the new reversible full adder.

VI. Discussion and Comparison Results

The simulator tool and simulation parameters are presented in the first subsection, subsection 2 indicates the simulation result of the new reversible gate and the last subsection expresses the analysis result of the proposed 1-bit reversible full adder.

1. Simulation tool and parameters

QCA Designer is provided by a group of researchers at the University of British Columbia to design and simulate quantum dot cellular automata technology. This tool allows its users to quickly design their structures, the QCA Designer supports both crossover and multi-layer overlays. In this research, all reversible structures are approved by QCA Designer Version 2. 0. 3. This tool has two simulation engines which called the Bistable Approximation and Coherence Vector. The bistable approximation engine calculates the mode of the QCA cells using a time independent strategy and Kink Energy equation. In addition, the simulation time on this simulator is much lower than the coherence vector engine. In this work, the bistable approximation engine is used and the amounts of its parameters are shown in Table 8.

TABLE VII
Bistable Approximation Parameter Model

Parameters	Value
Cell size	18*18 nm^2
Number of Samples	16000
Convergence Tolerance	0.001000
Radius of Effect	65.000000 nm
Relative Permittivity	12.900000
Clock High	9.800000e-022
Clock Low	3.800000e-023
Clock Shift	0.000000e+000
Clock Amplitude Factor	2.000000
Layer Separation	11.500000
Maximum Iterations Per Sample	100

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2. Simulation of the New Reversible Gate

The comparison result of the proposed reversible gate is demonstrated in Figure 10. According to Table 8, the performance analysis of the proposed reversible structure is considered in terms of number of cells, occupied area and the latency. It was observed that the proposed structure has improved about 70.32% in the number of cells, 81.08% in the occupied area and 94.38% in cost value as compared to the Fredkin gate that offered in [43]. Compared to the best design of the QCA RUG gate in [23], the improvements of the proposed structure are 75.42%, 84.78% and 98.12% in number of cell, occupied area and cost value, respectively. In comparing with the QCA reversible RM gate design in [48], the improvements in number of cell, occupied area and cost value are 67.41%, 72% and 90.87%, respectively. Also, 18.88%, 22.22% and 36.91% enhancements over the high efficiency design in [23] design in terms of number of cell, occupied area and cost value, respectively. Finally, based on the simulation results, the proposed reversible gate is better than the other investigated gates in cell count. As well as, the

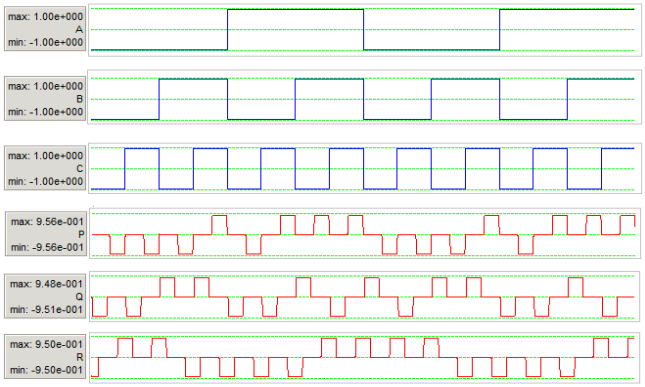

Fig. 11. Simulation results of the new reversible gate.

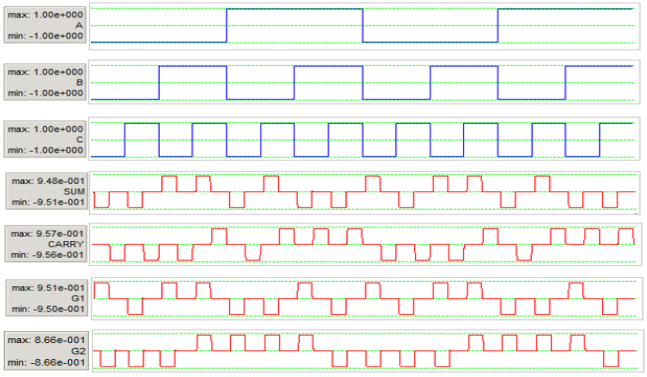

Fig. 12. Display of the input - output waveforms for the proposed QCA 1-bit reversible full adder.

The cost function of the proposed gate is decreased. Therefore, the lowest average number of reversible gates for designing our structure shows that its performance is great.

TABLE VIII
COMPARISON OF THE VARIOUS REVERSIBLE GATES IN QCA TECHNOLOGY

Reversible Gate	Implementation structures in QCA Designer				Cost
	Cell Count	Area (μm^2)	Latency (CLK)	Method of Wire-Crossing	
Fredkin [43]	246	0.37	1	Coplanar	91.02
New Gate 1 [49]	147	0.16	1	Coplanar	23.52
RUG [44]	297	0.46	2	Coplanar	273.24
RM [45]	224	0.25	1	Coplanar	56
NRG [10]	90	0.09	1	Coplanar	8.1
PRG [20]	146	0.14	1.25	Coplanar	25.55
Proposed	**73**	**0.07**	**1**	**Coplanar**	**5.11**

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TABLE IX
INVESTIGATION DESIGNS OF THE VARIOUS QCA 1-BIT REVERSIBLE FULL ADDER ARCHITECTURES

Structure	Cell Count	Area (μm^2)	Latency	Constant input	Garbage output	Wire-crossing type	Type of design
Presented in [51]	396	0.65	4	1	2	Multilayer Crossing	Reversible
Presented in [52]	371	0.35	1.5	0	3	Multilayer Crossing	Reversible
Presented in [50]	318	0.26	2	1	2	Multilayer Crossing	Reversible
Presented in [53]	513	0.57	4	0	6	Coplanar (clocking based)	Reversible
Presented in [41]	375	0.37	4.75	2	3	Multilayer Crossing	Reversible
Presented in [20]	562	0.70	1.25	1	6	Coplanar (clocking based)	Reversible
Our design	**115**	**0.116**	**1**	**1**	**2**	**Coplanar (clocking based)**	**Reversible**

VII. CONCLUSION

In this work, a 2-input XOR gate has been improved and a novel 3×3 reversible gate designed with the modify XOR gate that has the universal capability. Then, we executed each one a 13 standard logic function with this reversible gate. In addition, the new reversible gate can use for design various reversible combinational digital circuits such as the 1-bit comparator and 1-bit full adder. The proposed reversible gate has been improved main parameters like as number of cells, occupied area and latency. Therefore, all designed structures are improved in comparison with the other similar works. These circuits have a single layer without using rotated cells, so they can be simply used in designing different digital circuits based on QCA technology. The suggested designs are examined via the QCA Designer Version 2. 0. 3. Finally, for future research, the proposed reversible gate can be utilized for adder/subtractor designing and arithmetic and logic unit (ALU).

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