Design and Simulation of a Low Power RF Front-End for Short Range Outdoor Applications

Hamid Yadegar Amin, Farshad Piri and Ece Olcay Güneş

Dept. of Electronics and Communications Engineering, Istanbul Technical University, Istanbul, Turkey

*Corresponding Author's E-mail: amin@itu.edu.tr

Abstract

This paper presents a low power low voltage RF front-end for short range outdoor applications, meeting the IEEE 802.15.4 standard of 2.4 GHz for ZigBee systems. The design includes a two stage low power LNA with an integrated differential power splitter. Also, a low power, low voltage mixer is implemented to maintain the power specification of the design. The whole system has an almost 2.76mW power dissipation and is supplied by 1.2 V voltage source. The design accomplished in TSMC 180nm CMOS process. According to the simulation results acquired by Cadence Virtuoso, the design owns 22 dB conversion gain and 4.8 dB noise figure with IIP3 of -6.3 dBm.

Keywords: RF front-end; Low noise amplifiers; low power mixer; ZigBee; wireless sensors; solar cells.

1- Introduction

Low data rate wireless sensor networks (LR-WSN) are indisputable part of the smart systems. These networks are applicable in numerous applications such as smart farming for environmental sensing, military tracking and bio-sensing systems. LR-WSNs are made out of hundreds or even thousands of nodes. Each node works autonomously and is in communication with one or multiple nodes through a mesh network. Considering the high quantity of nodes, the power consumption of whole system comes into prominence. In this regard various low power protocols under IEEE 802.15.4 standard is defined. The ZigBee [1], protocol is defined under the mentioned standard for short range low data rate and low power applications. This protocol is specified to operate in ISM band, 2.4 GHz as the worldwide standard; 784 MHz in China, 868 MHz in Europe and 915 MHz in the USA and Australia. Data rates vary from 20 Kbit/s (868 MHz band) to 250 Kbit/s (2.4 GHz band) [2-3]. In ZigBee protocol, each node is a short range low power RF transceiver which is made out of some sub blocks as shown in Fig.1. Among other sub-blocks such as base band mixed signal and digital processing, the RF-front end block is the most power consumer block. High power front-ends cannot be supplied by energy harvesting systems such as solar cells or RF power scavenging systems [4].

![Fig. 1: Simplified block diagram of the receiver.](image-url)
On the other hand, due to the numerous number of nodes, using non-rechargeable batteries is not practical. Therefore, there has been tremendous effort to diminish power consumption of the ZigBee transceivers [5-8] to accommodate energy harvesting systems. This work presents a 2.76mW CMOS RF-Front end in 180nm TSMC process accommodate a single solar cell (~20mm²) [9]. The design includes a two stage cascaded single ended LNA. Also a low power mixer is utilized to accomplish all system with power consumption lower than 2.76mW. The design procedure and implemented topologies are explained in Section II. Section III, presents the simulation results and comparison to the previous designs.

2- Architecture and specifications

Thanks to using fewer blocks the direct conversion technique seems to fit better to low power-low voltage applications compared to the super heterodyne receivers. However, rendering time-varying DC offset, due to the nonlinearity of the mixer [10], and also, degraded noise specification restrict its application. In this regard, the IF is converted to a band near to the DC where the filters and blocks could be designed efficiently and far enough from DC band in which DC offset and flicker noise is problematic [11]. In this paper, the input RF signal is down converted to the base-band by means of a low-IF architecture as shown in Fig.2. In designing LNA, the single ended structure is chosen which is appropriate to the single input port coming from the antenna. Also, due to the low voltage and low noise specifications, the design is presented as the cascaded common source LNA with inductive source degeneration. Also, to address the low power specification, the LNA is merged with the mixer block in a current reusing fashion instead of using the differential power splitter (DPS).

![schematic of proposed RF front-end.](image)

To have a reflection-less power transformation, the input impedance of the Front-End should match to the antenna. The input impedance, $Z_{in}$ is calculated using small signal analysis in Eq. (1).

$$
Z_{in} = j\omega L_{s} + \frac{1}{j\omega (C_{g}+C_{p})} + \frac{L g_{m}}{(C_{g}+C_{p})}
$$

(1)

Where, $C_{p}$ is the gate-source capacitor of M1. The $C_{p}$ is utilized to get optimum input noise matching [12]. As seen in Fig.2, a C-C-L matching network (CM1, CM2 and LM3) is used as DC block which also cancels out the imaginary part of the $Z_{in}$. Also, $L_{s}$, $g_{m}$ and capacitors are contributing to match real of the $Z_{in}$ to 50 ohm. The $L_{s}$ inductors, are implemented in bond wires to include the parasitic effect of the package pins. Fig.3, presents small signal analysis of the LNA block when M3 and M4 are
disconnected and M2 is loaded only by Rd. The LNA has a 15dB gain and below -10dB reflectance over desired frequency band. To diminish chip area size, its input is matched to the 50ohm input port using the least number of inductors. The LNA has shown 4.2 dB noise after a noise optimization. As shown in Fig.2, a single balanced mixer is merged to the LNA to use the same DC bias current. Transistors M3 and M4 provide gm of the mixer. Biasing those transistors in sub-threshold region leads to get higher gm which consequently, contributes to higher conversion gain and improve noise and linearity [13].

![Fig. 3: Small signal analysis including S-parameter and Noise factor.](image)

The mixer could be loaded by inductive or active loads as well. However, using inductive loads costs to extra chip size and active loads, also, impose more noise to the system. Therefore, a resistive load is preferred overlooking the headroom limitations. Table.1 and Fig.4, give the component value of the design and layout view respectively.

![Fig. 4: Layout view of the designed Front-End with area of 1518um-600um.](image)

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>CM1</td>
<td>4 pF</td>
<td>Cg</td>
<td>2 pF</td>
</tr>
<tr>
<td>CM2</td>
<td>2 pF</td>
<td>M2</td>
<td>140u / 0.18u</td>
</tr>
<tr>
<td>LM3</td>
<td>4.9 nH</td>
<td>M3</td>
<td>140u / 0.18u</td>
</tr>
<tr>
<td>Cp</td>
<td>790 fF</td>
<td>M4</td>
<td>140u / 0.18u</td>
</tr>
<tr>
<td>M1</td>
<td>120u/0.18u</td>
<td>Rd</td>
<td>500 Ω</td>
</tr>
<tr>
<td>Ld</td>
<td>7.16 nH</td>
<td>Ic1/Ic2</td>
<td>2 m / 0.3 m</td>
</tr>
</tbody>
</table>
3- Simulation results

The simulations are accomplished in Cadence Virtuoso simulator and all components are taken from TSMC 180nm CMOS library. Fig.5 presents reflected power and noise figure of the design. Where, the output port is attached to the Vo,.

Fig. 5: Reflection power and Noise analysis of the designed Front-End.

As depicted in Fig.5 the design has shown -11 dB reflection and 4.8 dB noise factor at 2.4 GHz. The test bench takes all components and bond wires from TSMC CMOS library. In this paper, the IF frequency is determined as 300 MHz as it is known, the conversion gain is the power ratio of the IF harmonic to the input harmonic. During simulations the RF input frequency is defined at 2.4 GHz with power of −30 dBm. Also, for LO the frequency and power level are specified as 2.1 GHz and 0 dBm. Fig.6 demonstrates the power harmonics of the design. As it is seen the system shows an almost 22 dBm power gain at the IF frequency.

Fig. 6: Output power spectrum of the designed Front-End.

The third order intermodulation intercept point (IIP3) is calculated by running a two-tone simulation. Fig.7, shows the simulated results. As it is seen in the Fig.7, IIP3 is found to be -6.3 dBm. The overall performance of the Front-Ends can be expressed by means of FOM (Figure of merit), Eq. (2).

\[
FOM = 20 \log_{10} \left( f_{\text{IF}} \right) + CG - NF + IIP3 - 10 \log_{10} \left( P_{\text{RF}} \right)
\]

(2)
Where, the frequency is normalized to 1 Hz. Conversion gain and noise factor are normalized to 1 dB. The IIP3 and dissipated power are normalized to 1dBm and 1mW respectively.

**Fig. 7:** IIP3 analysis of the designed Front-End.

### Conclusion

The design and layout of a low power CMOS front-end receiver for ZigBee applications is presented. Amplifying the received signals at 2.4 GHz and converting it to the IF band are accomplished by means of merged LNA and mixer to keep the chip area and consumed power as low as possible. Table 2, summarizes the simulation results and gives a comparison to the other previous works.

#### Table 2: RF Front-End performance comparisons.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>90 nm</td>
<td>180nm</td>
<td>180nm</td>
<td>130nm</td>
<td>180 nm</td>
<td>180 um</td>
</tr>
<tr>
<td>C-Gain (dB)</td>
<td>30</td>
<td>20.5</td>
<td>18</td>
<td>44</td>
<td>16.3</td>
<td>22</td>
</tr>
<tr>
<td>NF (dB)</td>
<td>7.5</td>
<td>13.2</td>
<td>8</td>
<td>3.75</td>
<td>11.5</td>
<td>4.8</td>
</tr>
<tr>
<td>IIP3(dBm)</td>
<td>-12.8</td>
<td>-7.8</td>
<td>-15</td>
<td>-31</td>
<td>-19</td>
<td>-6.3</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>5.64</td>
<td>1.08</td>
<td>8.2</td>
<td>25.2</td>
<td>6.74</td>
<td>2.76</td>
</tr>
<tr>
<td>Frequency (GHz)</td>
<td>2.4</td>
<td>2.4</td>
<td>2.4</td>
<td>2.4</td>
<td>2.4</td>
<td>2.4</td>
</tr>
<tr>
<td>FOM</td>
<td>189</td>
<td>187</td>
<td>173</td>
<td>182</td>
<td>169</td>
<td>194</td>
</tr>
</tbody>
</table>

### References


